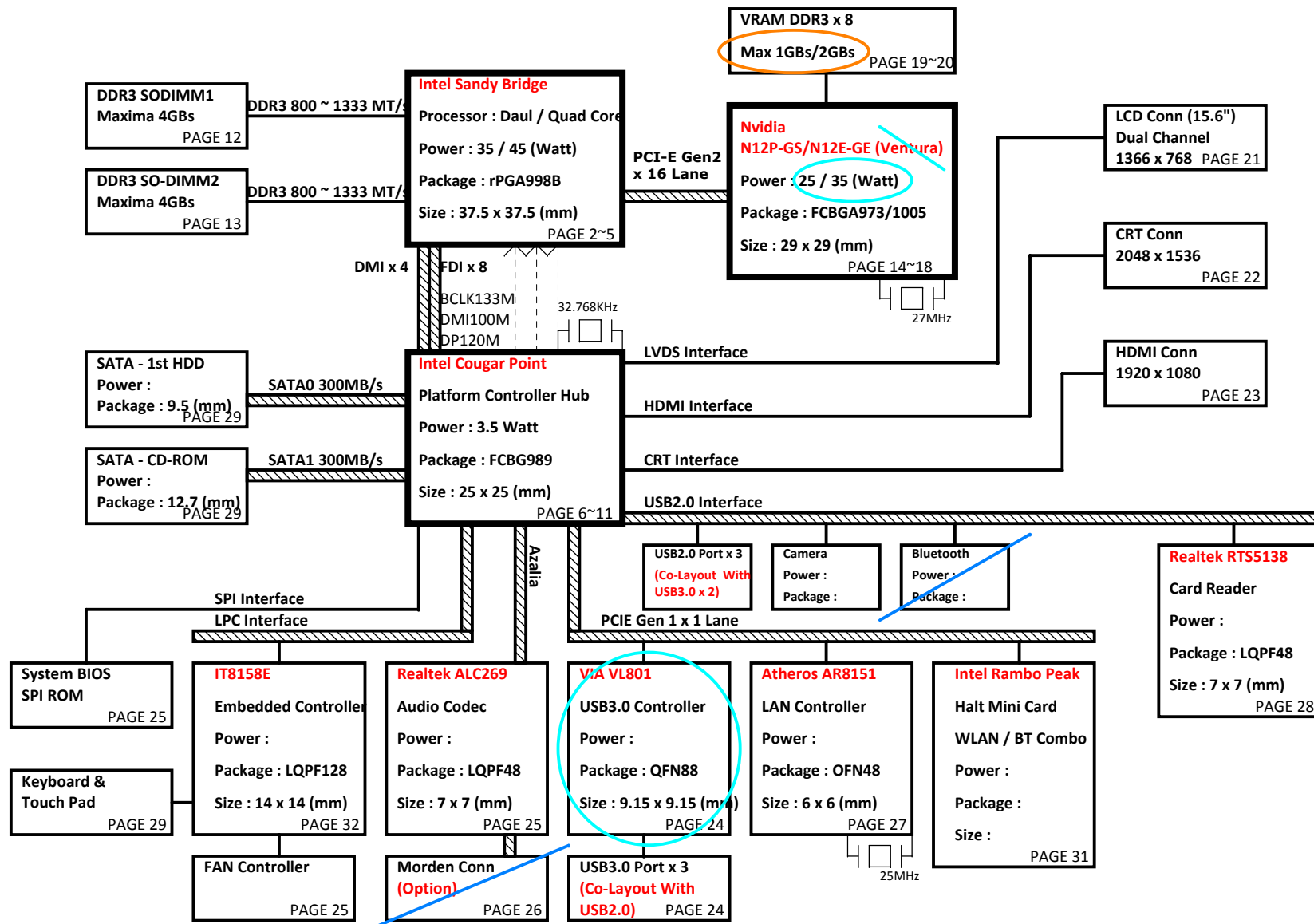


TWH (15.6") Intel Huron River Platform Block Diagram

01



PCB 6L STACK UP

- LAYER 1 : TOP
- LAYER 2 : SGND
- LAYER 3 : IN1(High)
- LAYER 4 : IN2(Low)
- LAYER 5 : SVCC
- LAYER 6 : BOT

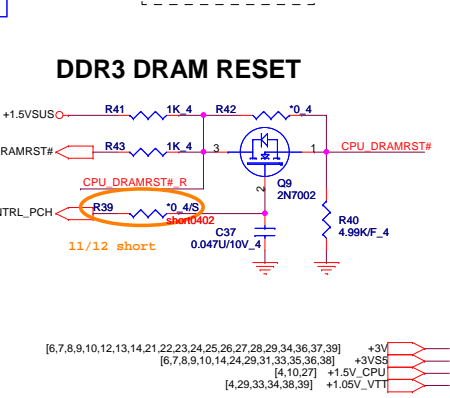
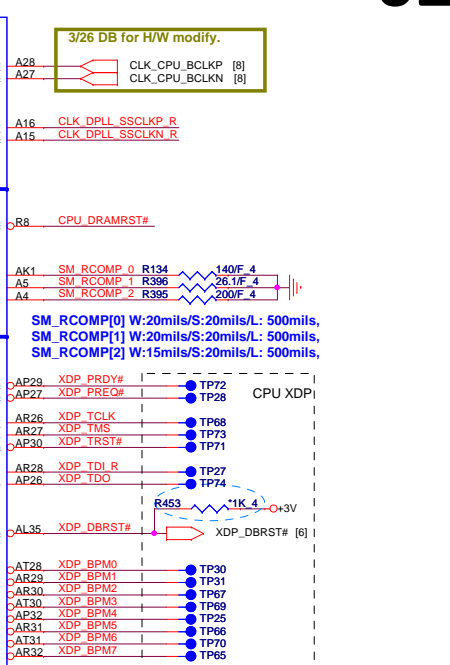
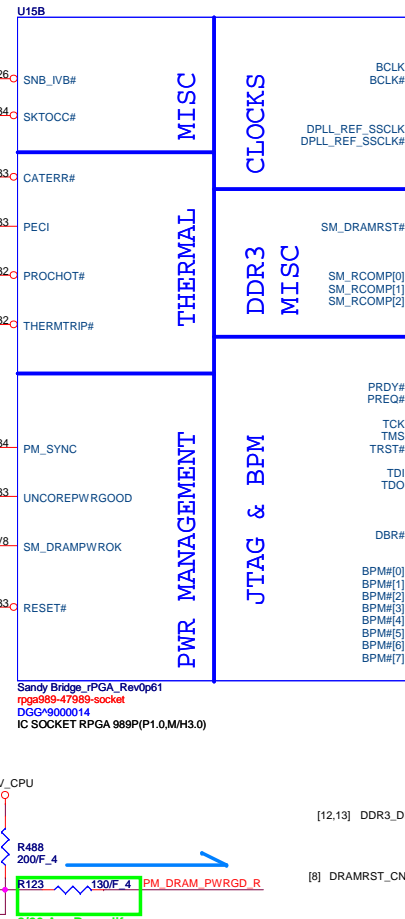
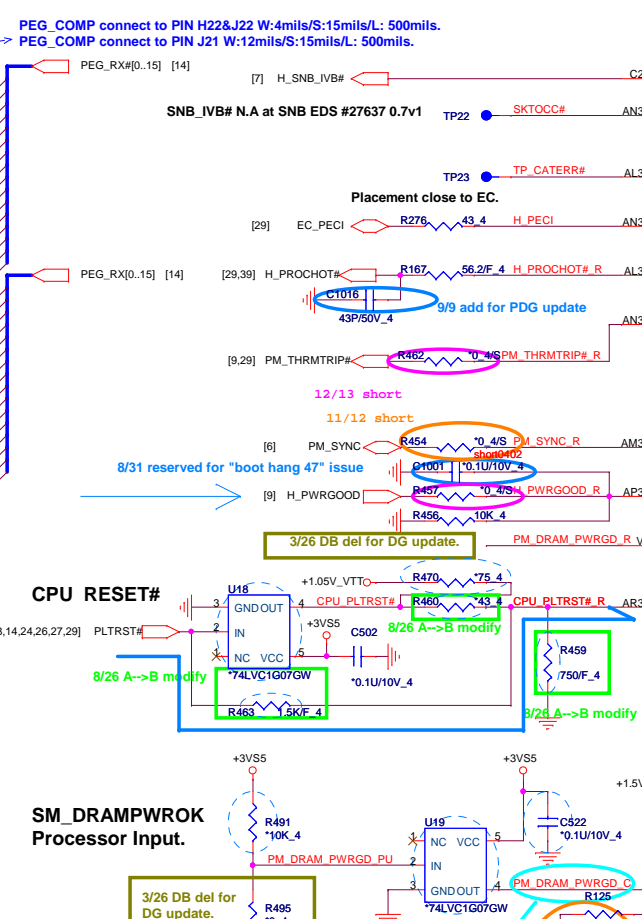
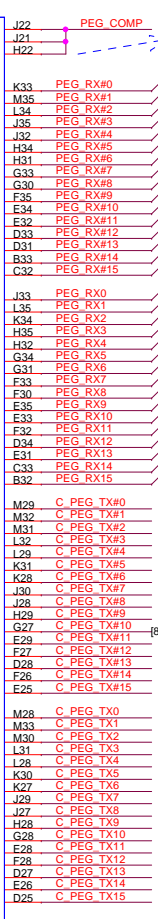
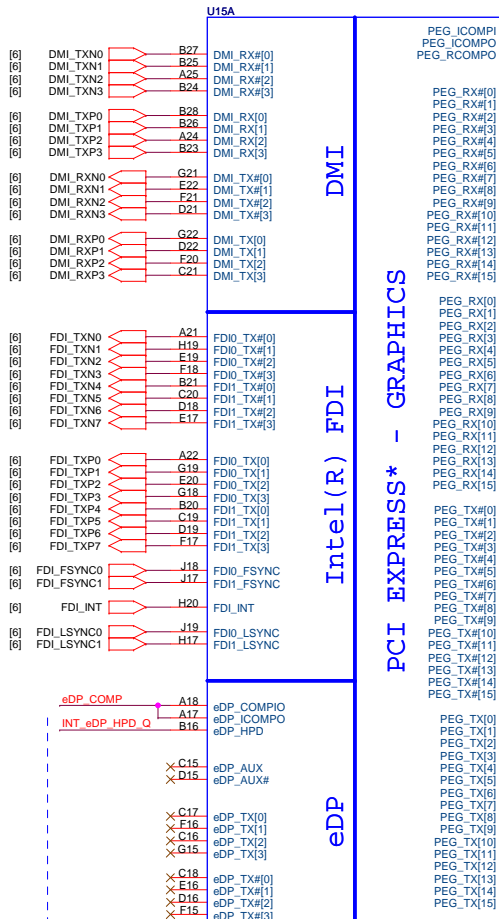
PCB 8L STACK UP

- LAYER 1 : TOP
- LAYER 2 : SGND
- LAYER 3 : IN1(High)
- LAYER 4 : IN2(Low)
- LAYER 5 : SGND1
- LAYER 6 : SVCC
- LAYER 7 : SGND2
- LAYER 8 : BOT

Power Source

- OZMicro OZ8681**
System Charge Power (+BATGCHG)
- P2806**
System Discharge Power (+1.5V/+3V/+5V)
- Rictech RT8205**
System Power (+3VPCU/+5VPCU/+3VS5/+5VS5)
- NCP6131/NCP5911/RT8209/G9334**
Processor Power (+VCC_CORE/+1.05_VTT/+VCCSA)
- Rictech RT8207**
System Memory Power (+1.5VSUS/+0.75V_DDR_VTT)
- Rictech RT8209/RT9025**
PCH Power (+1.05/+1.8V)
- OZMicro OZ8122**
DGPU Power (+VGACORE/+3.3V_GFX/+1.8_VGA/+1.5_GFX/+1.05_GFX)

	PROJECT : TWH Quanta Computer Inc.		
	Size A3	Document Number Block Diagram	Rev A
	Date: Tuesday, January 04, 2011	Sheet 1 of 40	



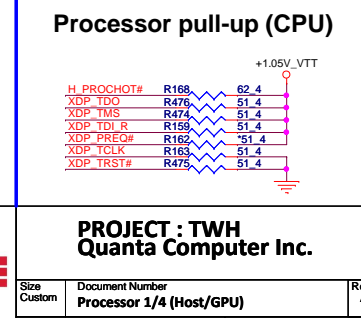
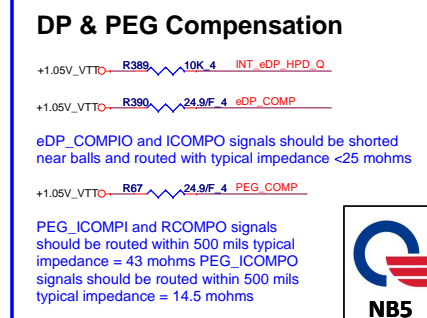
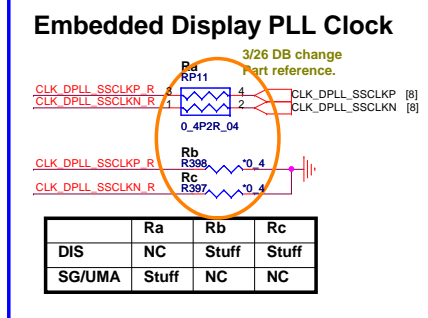
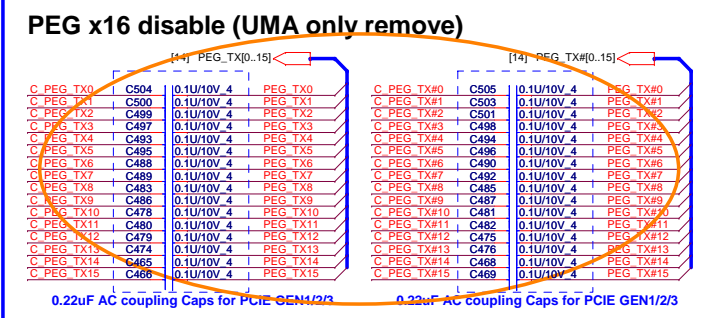
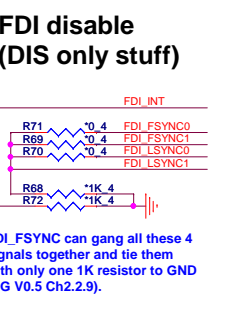
Sandy Bridge_rPGA_Rev0p61
rpgs989-47989-socket
DQG#9000014
IC SOCKET RPGA 989P(P1.0,MH3.0)

eDP_COMP connect to PIN A18 W:4mils/S:15mils/L: 500mils.
eDP_COMP connect to PIN A17 W:12mils/S:15mils/L: 500mils.

SM_DRAMPWROK Processor Input.
8/26 A->B modify
12/13 short
8/31 change to 0 ohm

Sandy Bridge_rPGA_Rev0p61
rpgs989-47989-socket
DQG#9000014
IC SOCKET RPGA 989P(P1.0,MH3.0)

[6,7,8,9,10,12,13,14,21,22,23,24,25,26,27,28,29,34,36,37,39] +3V
[6,7,8,9,10,14,24,29,31,33,35,36,38] +3VSS
[4,10,27] +1.5V_CPU
[429,33,34,38,39] +1.05V_VTT

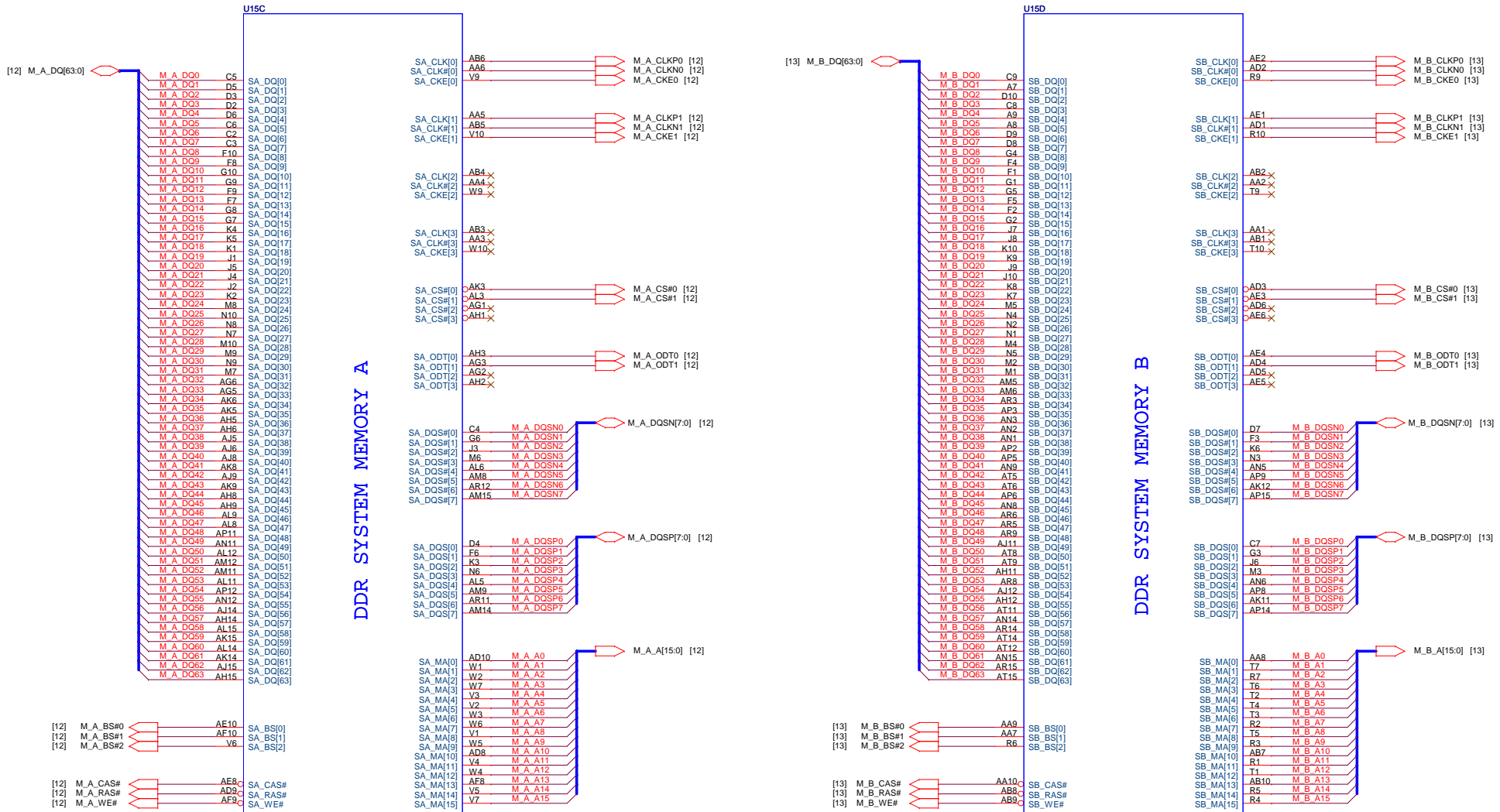


PROJECT : TWH
Quanta Computer Inc.

Size Custom Document Number Processor 1/4 (Host/GPU) Rev A

Date: Tuesday, January 04, 2011 Sheet 2 of 40

Sandy Bridge Processor (DDR3)



Sandy Bridge_rPGA_Rev0p61
 rpg989-47989-socket
 DGG-9000014
 IC SOCKET RPGA 989P(P1.0,M/H3.0)

Sandy Bridge_rPGA_Rev0p61
 rpg989-47989-socket
 DGG-9000014
 IC SOCKET RPGA 989P(P1.0,M/H3.0)

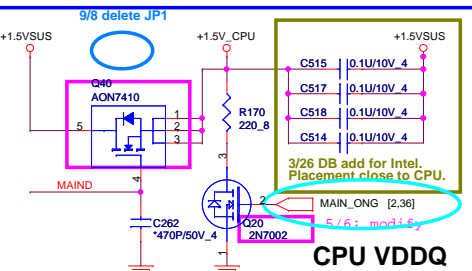
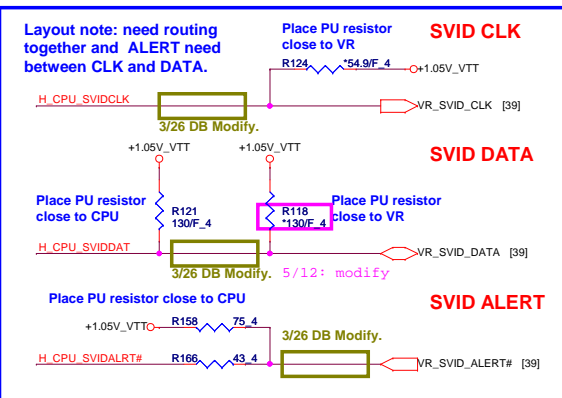
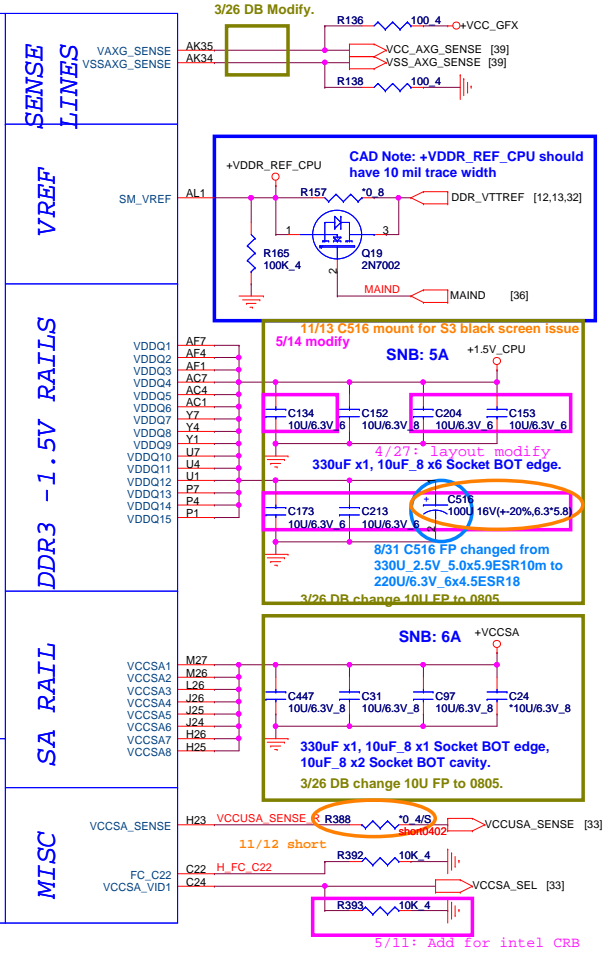
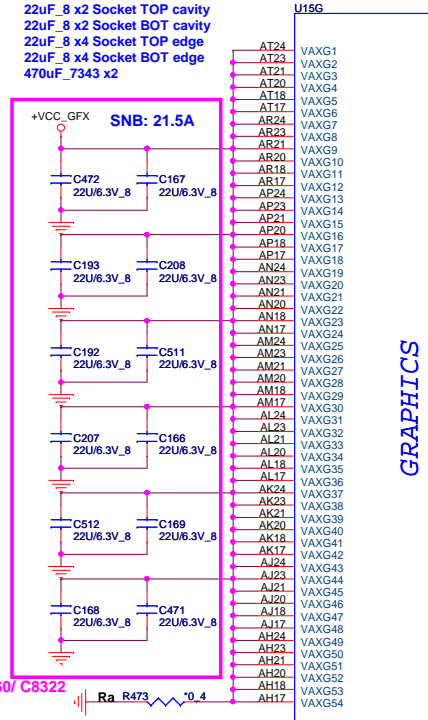
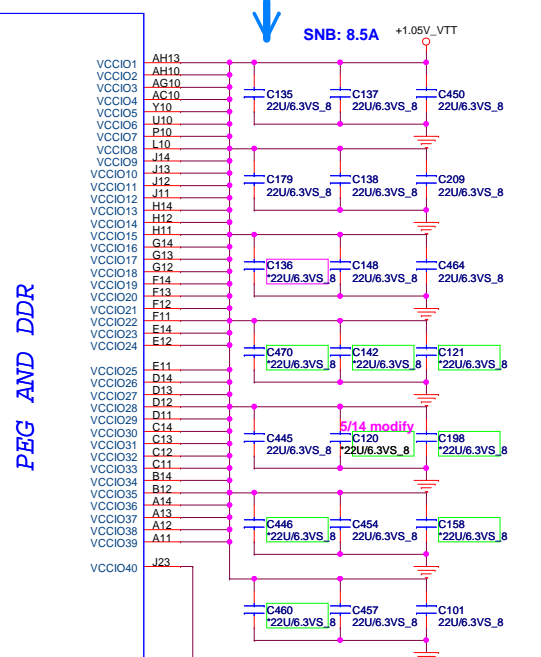
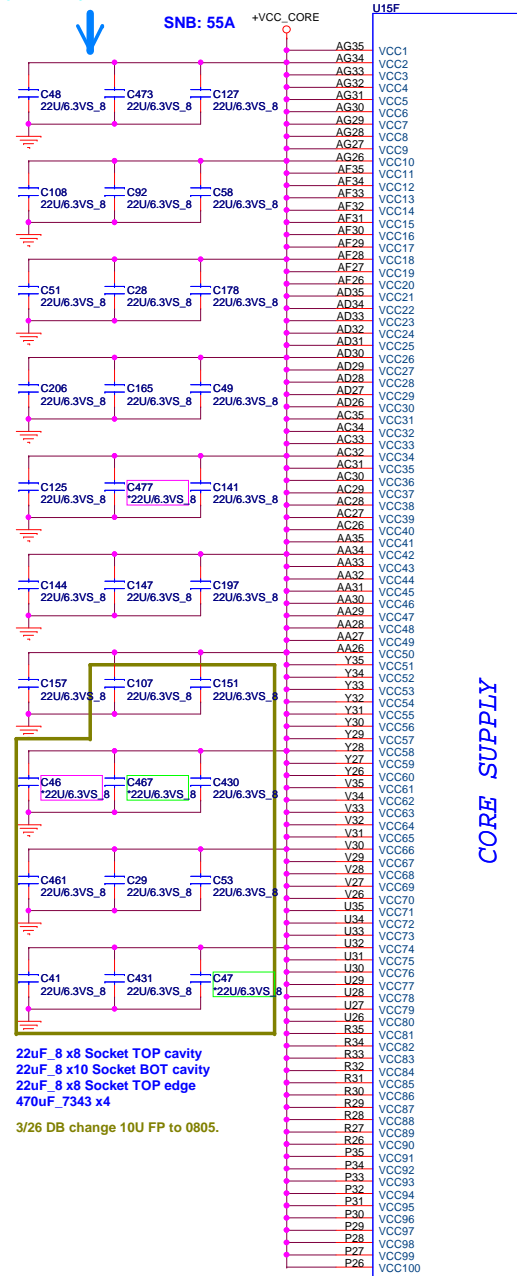
	PROJECT : TWH Quanta Computer Inc.		Rev A
	Size Custom Document Number Processor 2/4 (Memory)	Date: Tuesday, January 04, 2011 Sheet 3 of 40	

Sandy Bridge Processor (POWER)

Sandy Bridge Processor (GRAPHIC POWER)

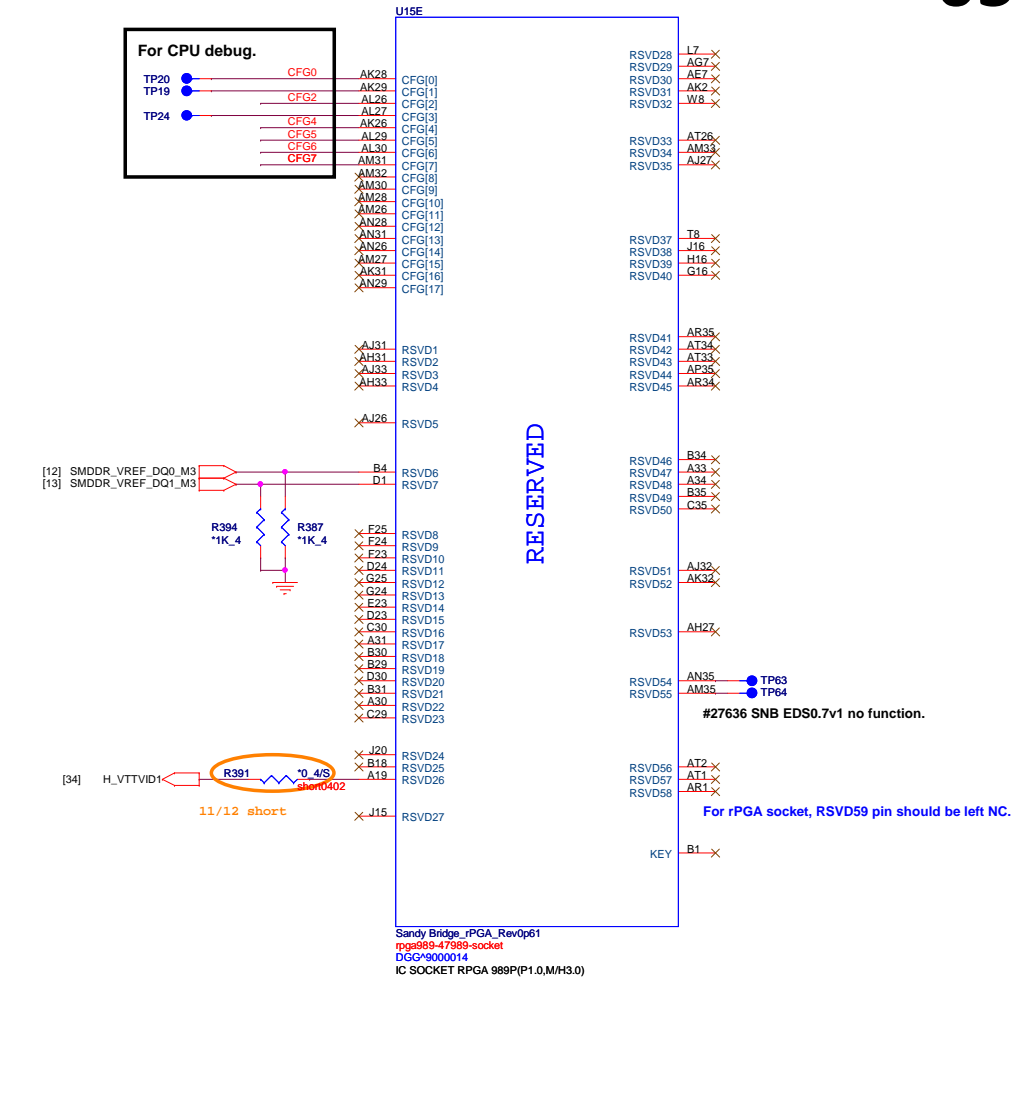
9/4 all of these 22uF/6.3V capacitors are replaced by 10uF/6.3V in BOM

9/4 all of these 22uF/6.3V capacitors are replaced by 10uF/6.3V in BOM



Sandy_Bridge_rPGA_Rev0p61
rpga989-47989-socket
DGG*9000014
IC SOCKET RPGA 989P(P1.0,M/H3.0)

[2,10,12,13,32,33,38] +1.5VSUS
[2,10,27] +1.5V_CPU
[2,29,33,34,38,39] +1.05V_VTT
[33] +VCCSA
[39,40] +VCC_GFX
[39,40] +VCC_CORE

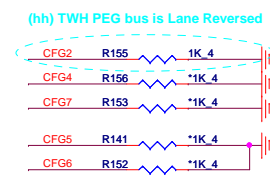


Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training

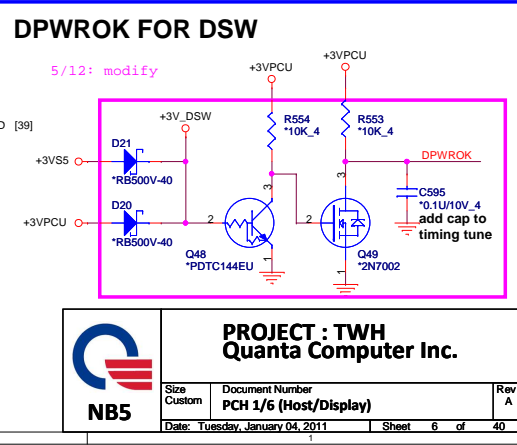
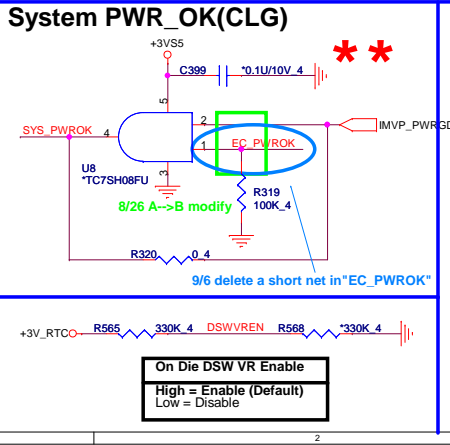
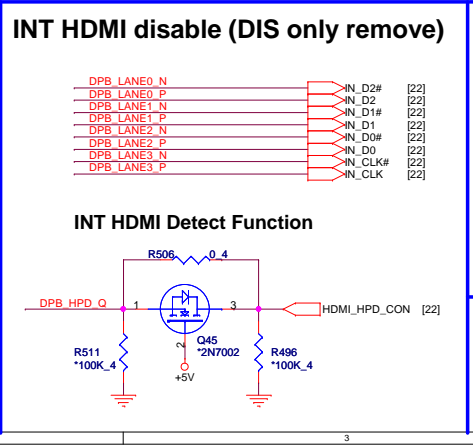
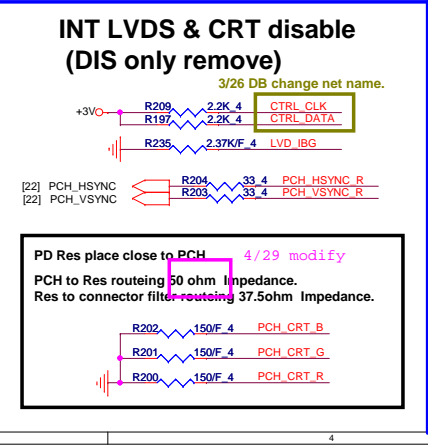
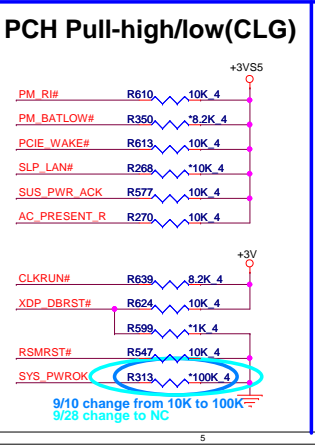
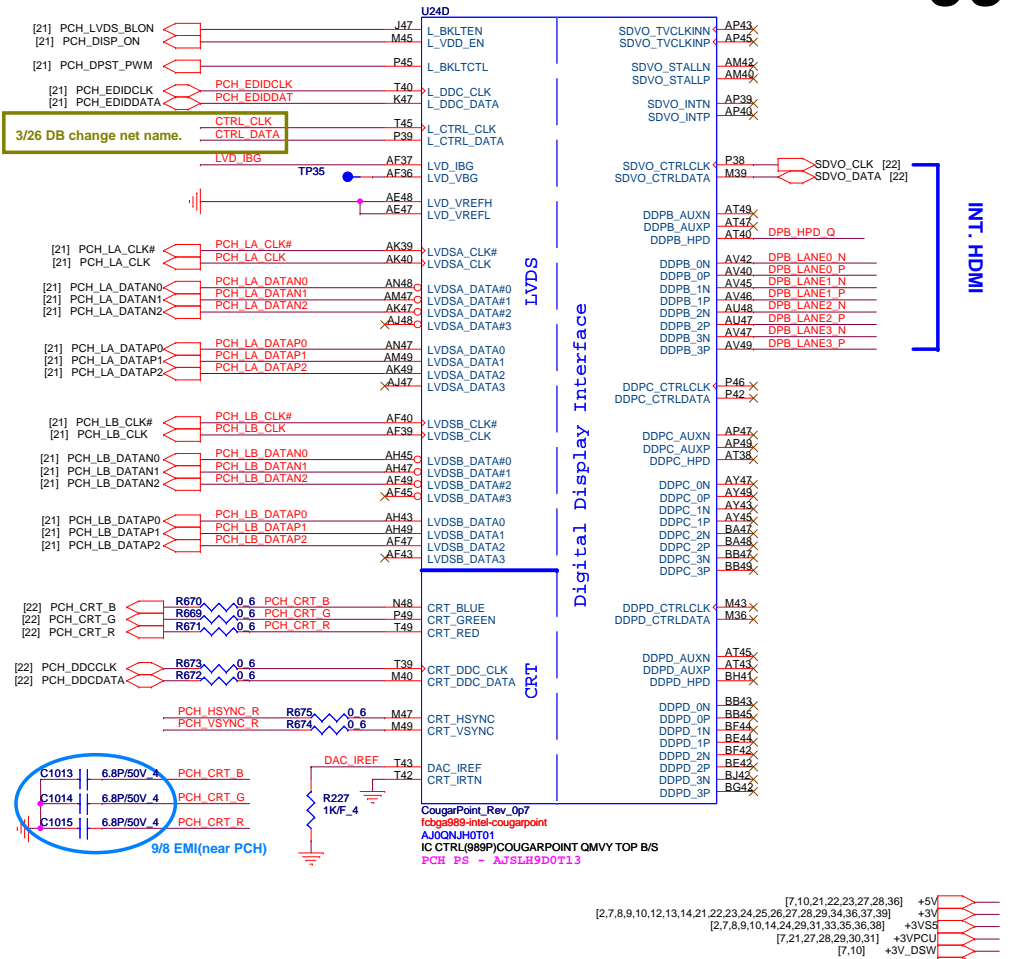
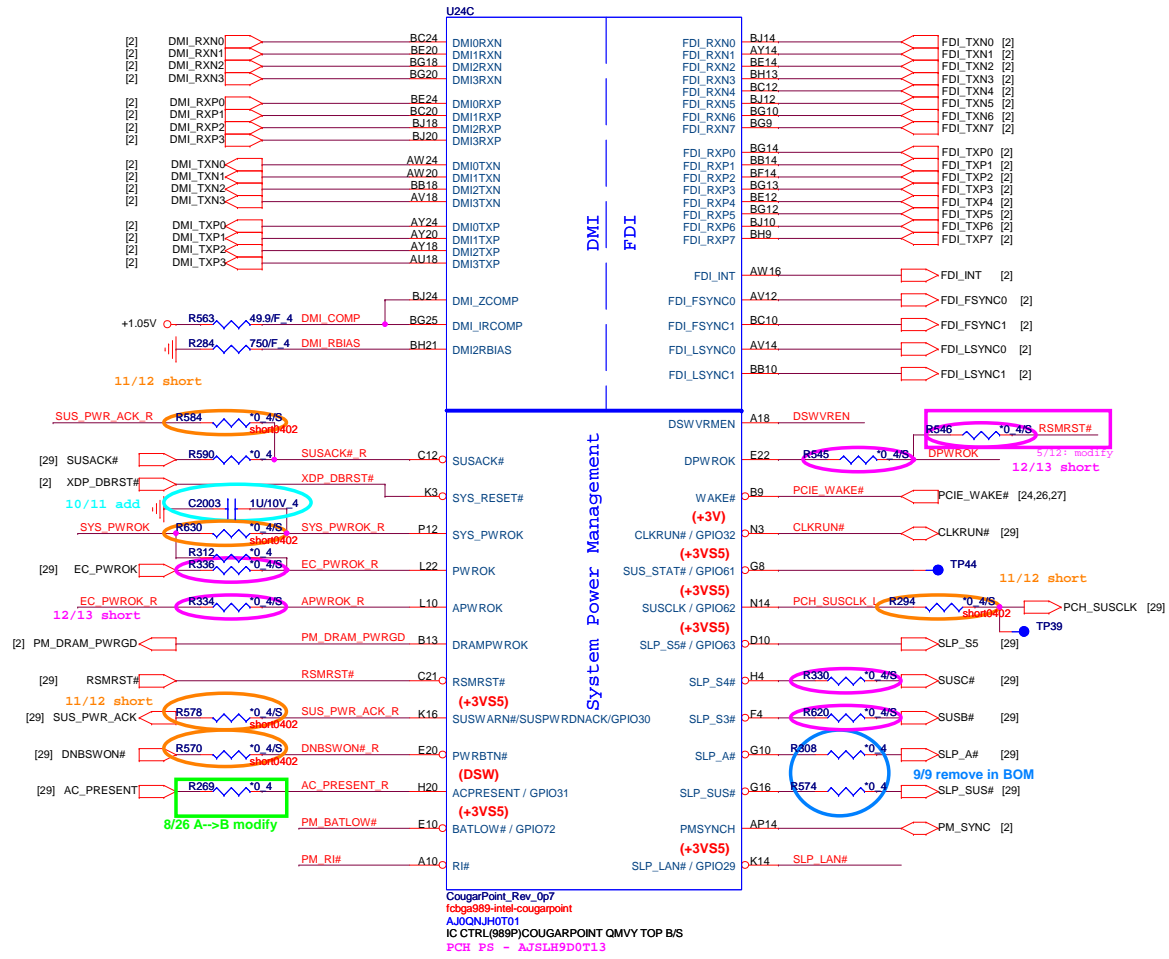
CFG[6:5] (PCIe Port Bifurcation Straps)
 11: (Default) x16 - Device 1 functions 1 and 2 disabled
 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
 00: x8, x4, x4 - Device 1 functions 1 and 2 enabled



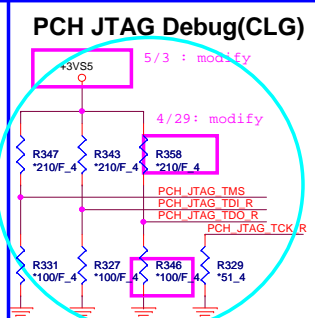
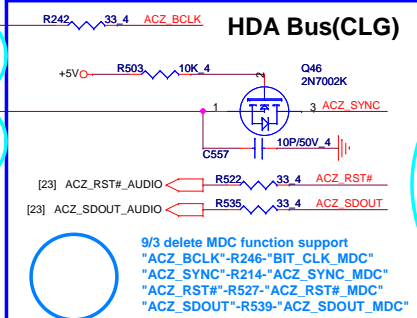
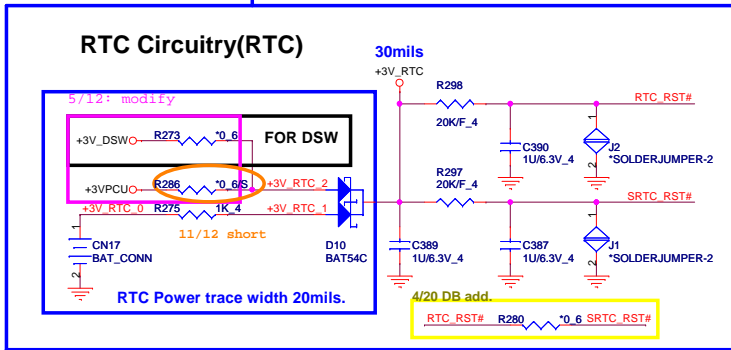
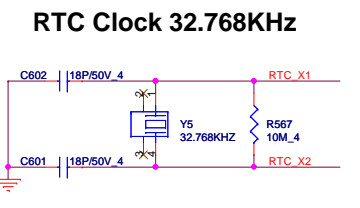
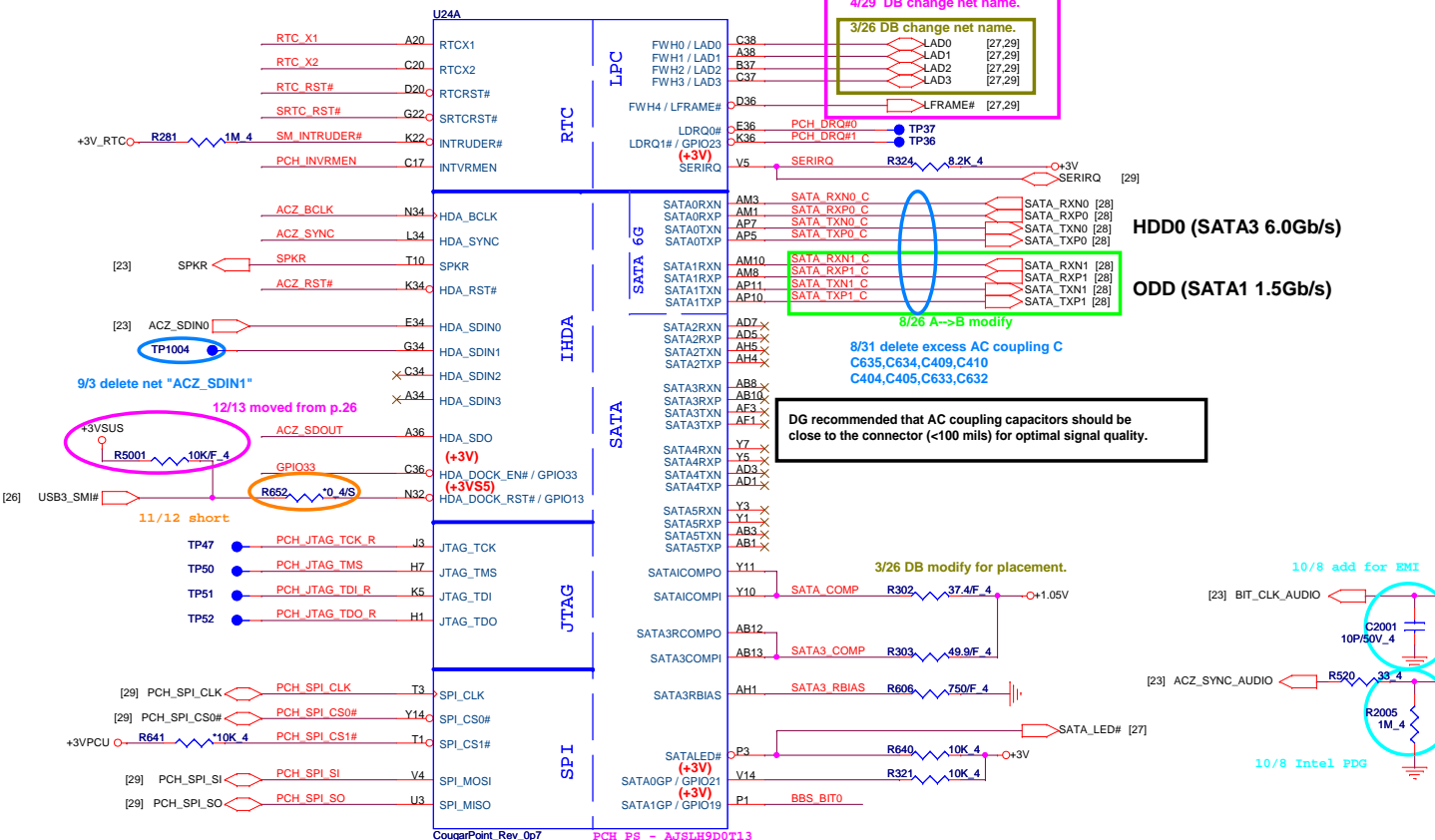
PROJECT : TWH
Quanta Computer Inc.

Size Custom Document Number Processor 4/4 (Ground) Rev A
 Date: Tuesday, January 04, 2011 Sheet 5 of 40

Sandy Bridge_rPGA_Rev0p61
 rpg989-47989-socket
 DGG*9000014
 IC SOCKET RPGA 989P(P1.0,M/H3.0)



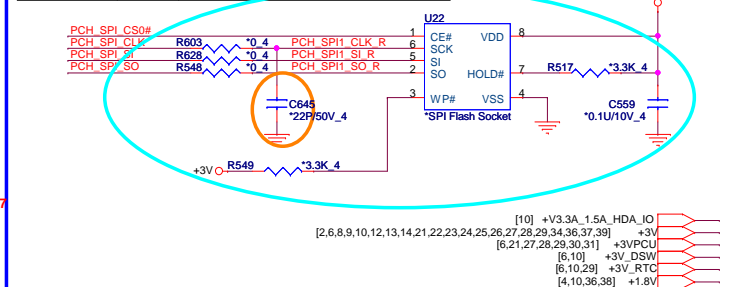
Cougar Point (HDA, JTAG, SATA)



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit									
SPKR	Different from Calpella No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode										
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)										
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up										
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)										
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"> <tr> <th>GNT1#</th> <th>GNT0#</th> <th>Boot Location</th> </tr> <tr> <td>1</td> <td>0</td> <td>SPI</td> </tr> <tr> <td>0</td> <td>1</td> <td>LPC</td> </tr> </table>	GNT1#	GNT0#	Boot Location	1	0	SPI	0	1	LPC	
GNT1#	GNT0#	Boot Location											
1	0	SPI											
0	1	LPC											
GPIO19	Different from Calpella Boot BIOS Selection 0 [bit-0]	PWROK	Should not be pull-down (weak pull-up 20K)										
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN									
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)										
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm 4/29 modify										
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V										
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K) 8/26 A-->B modify										
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)										
GPIO28	Different from Calpella On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)										
SPI_MOSI	ITPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable										

Vender	Size	P/N
EON	4MB	AKE39FNQ00 (EN25F32-100HIP)
Winbond	4MB	AKE391P0N00 (W25Q32BVSSIG)
Socket		DG008000031



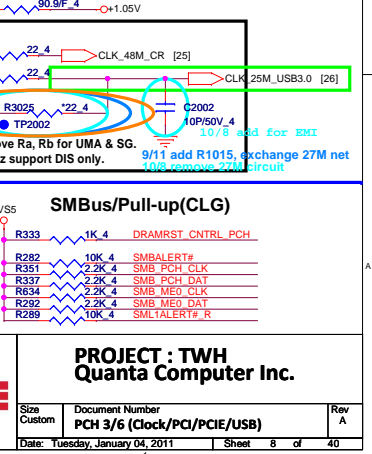
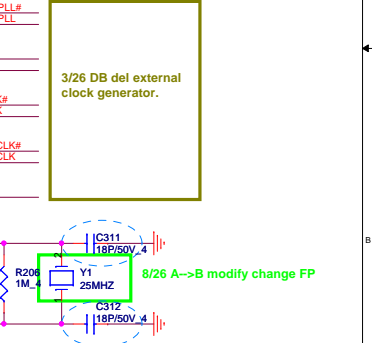
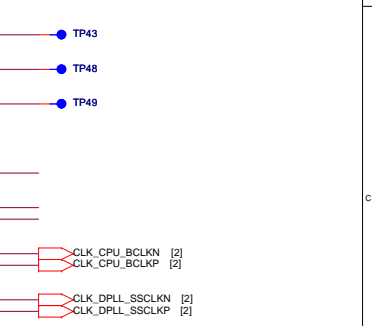
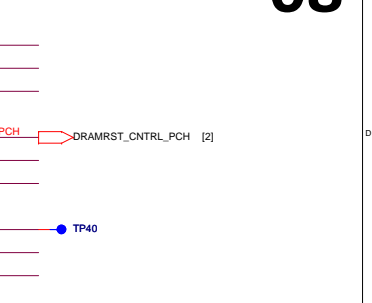
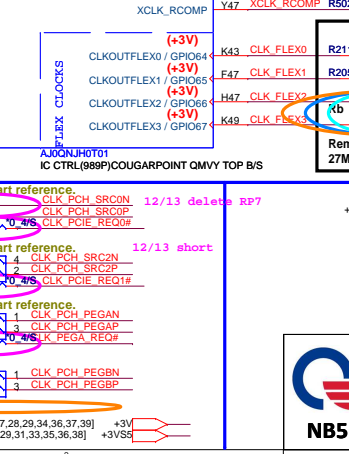
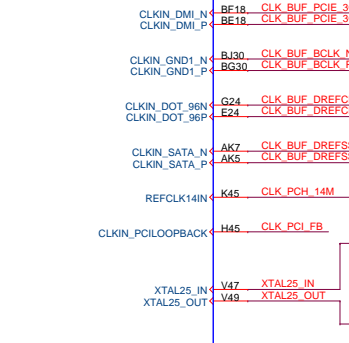
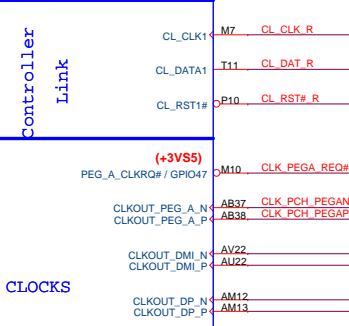
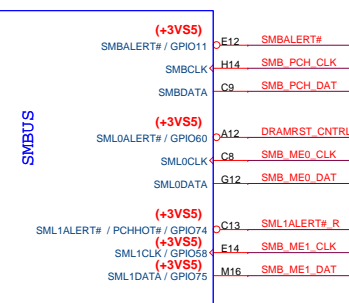
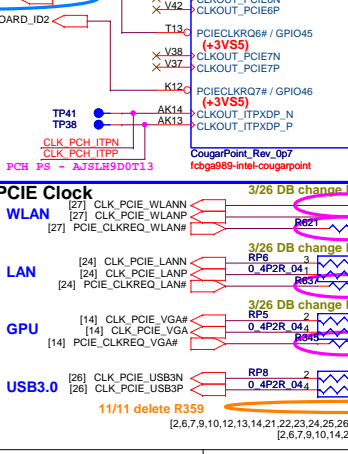
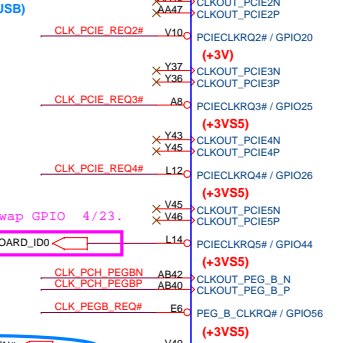
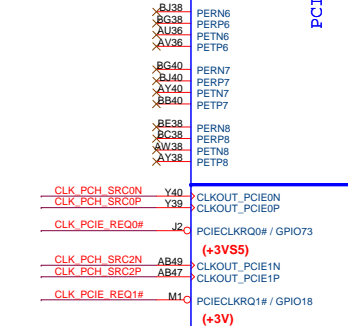
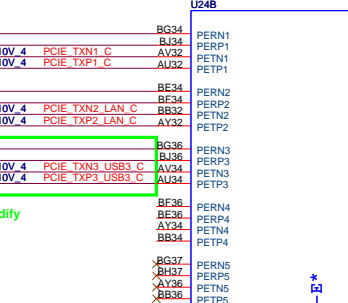
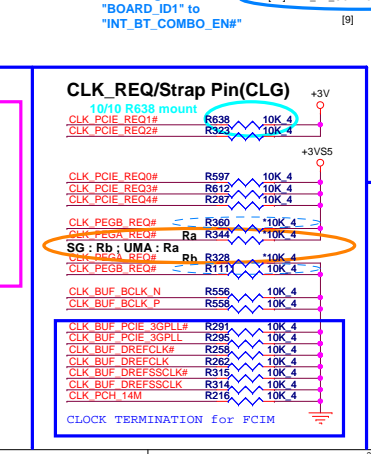
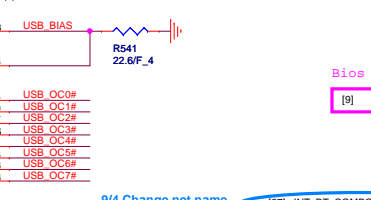
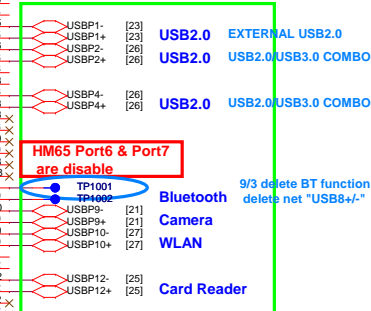
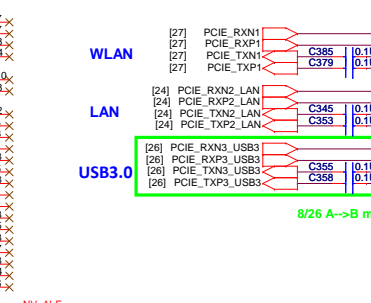
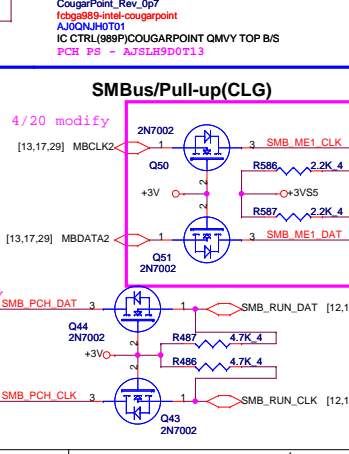
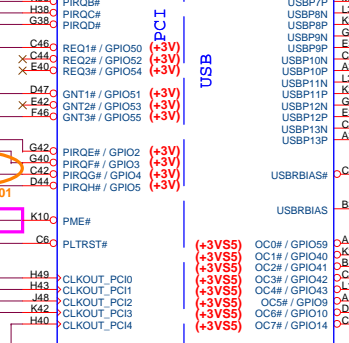
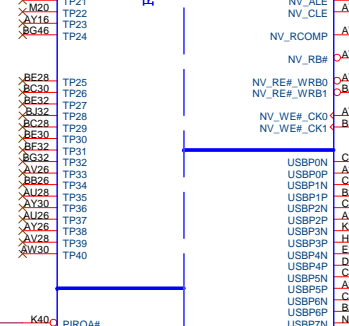
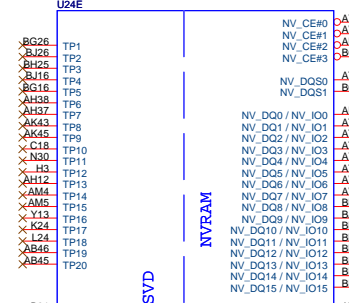
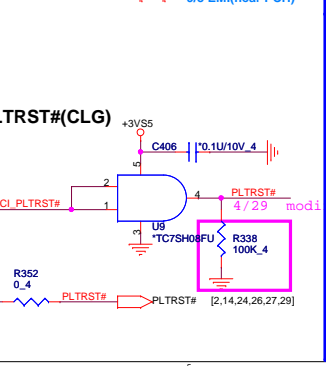
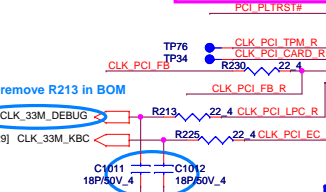
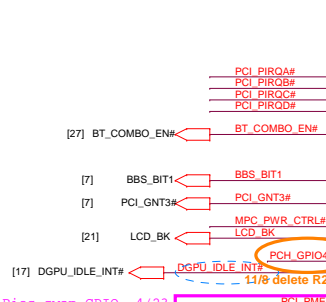
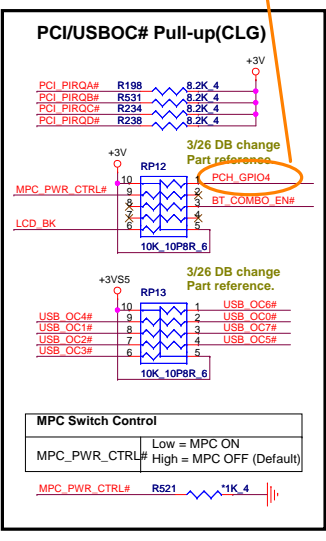
PROJECT : TWH Quanta Computer Inc.

Size Custom Document Number
PCH 2/6 (HDA/RTC/SATA/SPI)

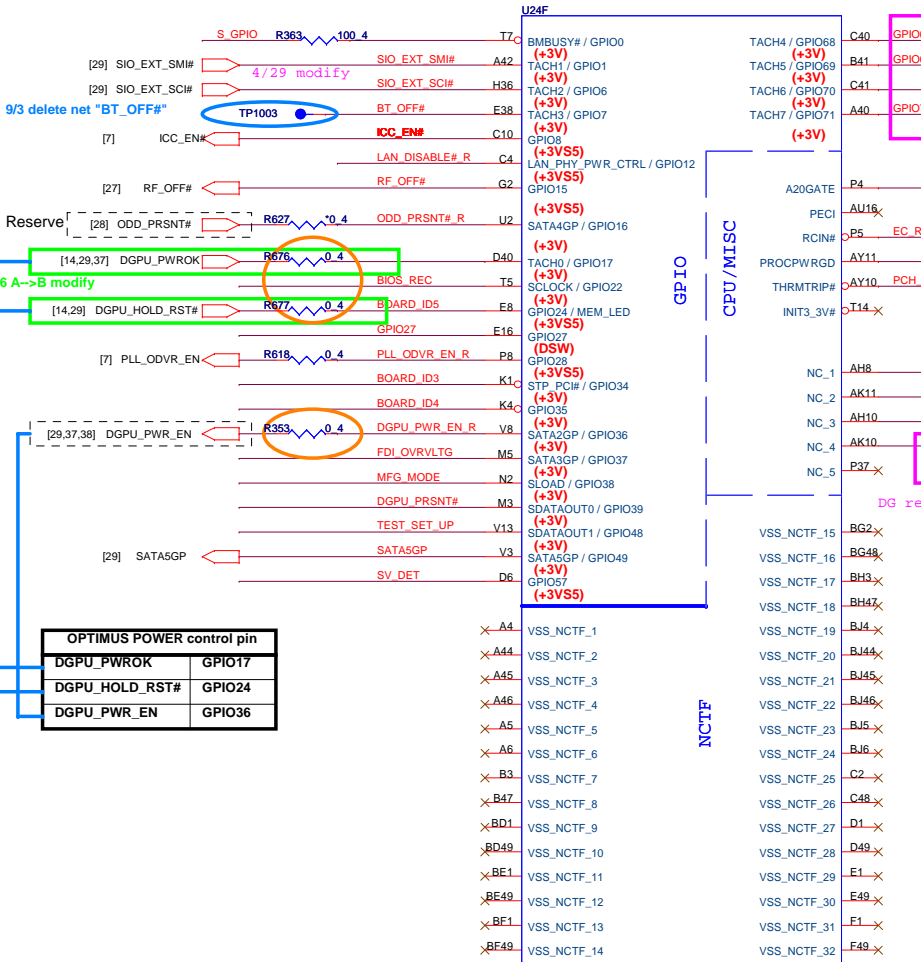
Date: Tuesday, January 04, 2011 Sheet 7 of 40

Cougar Point-M (PCI,USB,NVRAM)

Cougar Point-M (PCI-E,SMBUS,CLK)



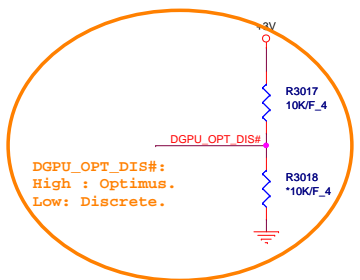
Cougar Point (GPIO,VSS_NCTF,RSVD)



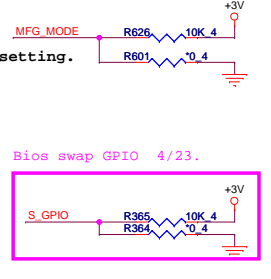
OPTIMUS POWER control pin	
DGPU_PWROK	GPIO17
DGPU_HOLD_RST#	GPIO24
DGPU_PWR_EN	GPIO36

CougarPoint_Rev_0p7 IC CTRL(989P)COUGARPOINT QMVTOP B/S
 fcbgs989-intel-cougarpoint
 AJQJNH0T01 PCH P5 - AJ5LH9D0T13

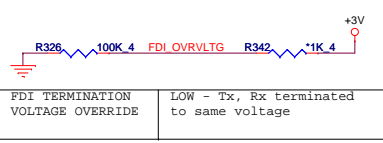
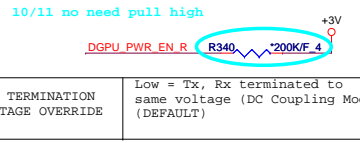
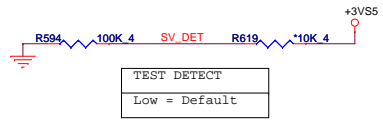
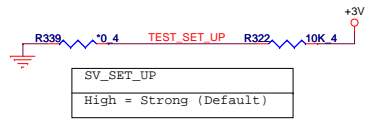
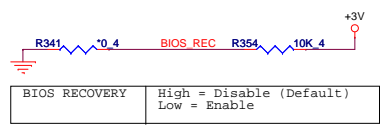
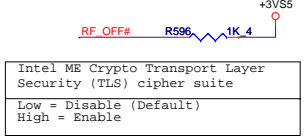
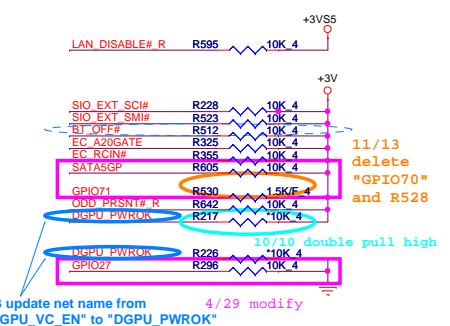
Clock Gen Power OK (CLG)



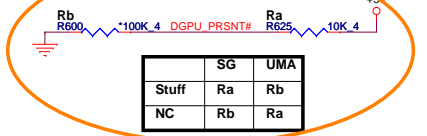
MFG-TEST



GPIO Pull-up/Pull-down(CLG)

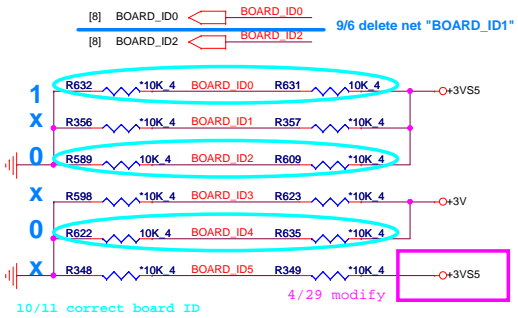


GFX Present



BOARD ID SETTING

Board ID	ID0	ID1	ID2	ID3	ID4	ID5
LG	0=LG 1=CB					
UMA/Dis.						0=UMA 1=Dis.
15.6"/14"			0=QLH/TWH 1=QLC/SWH			
MDC						0=YES 1=NO
Dobly					0=NO 1=YES	
Optiums						1=YES 0=NO

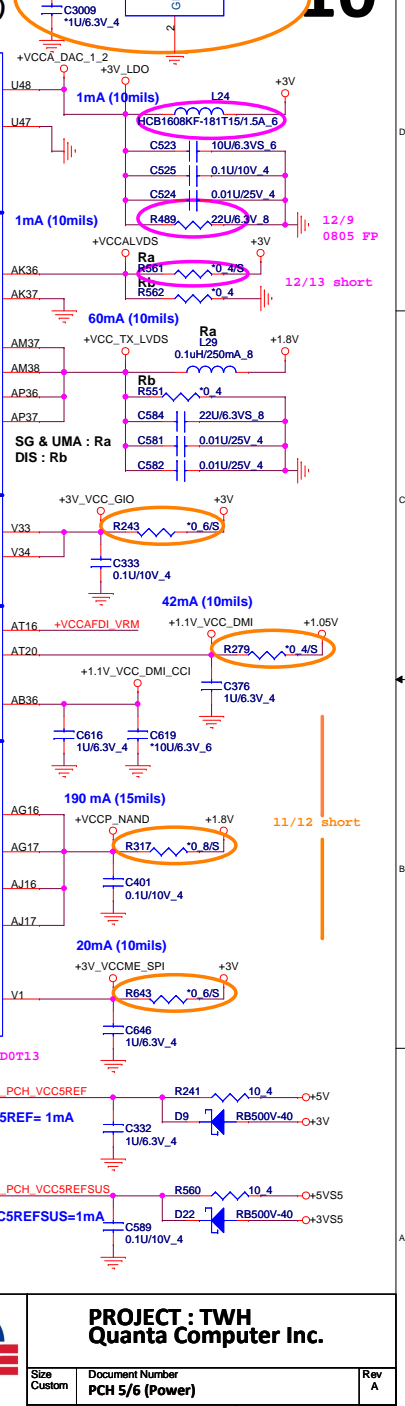
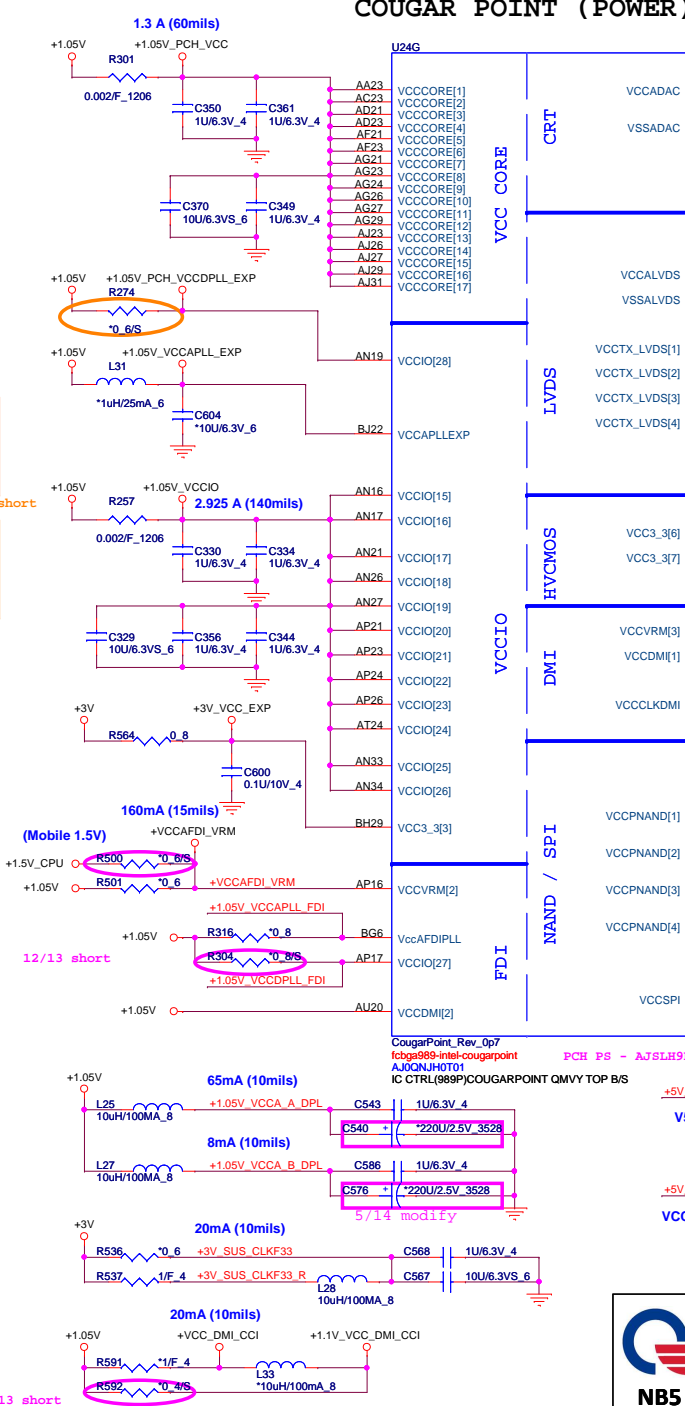
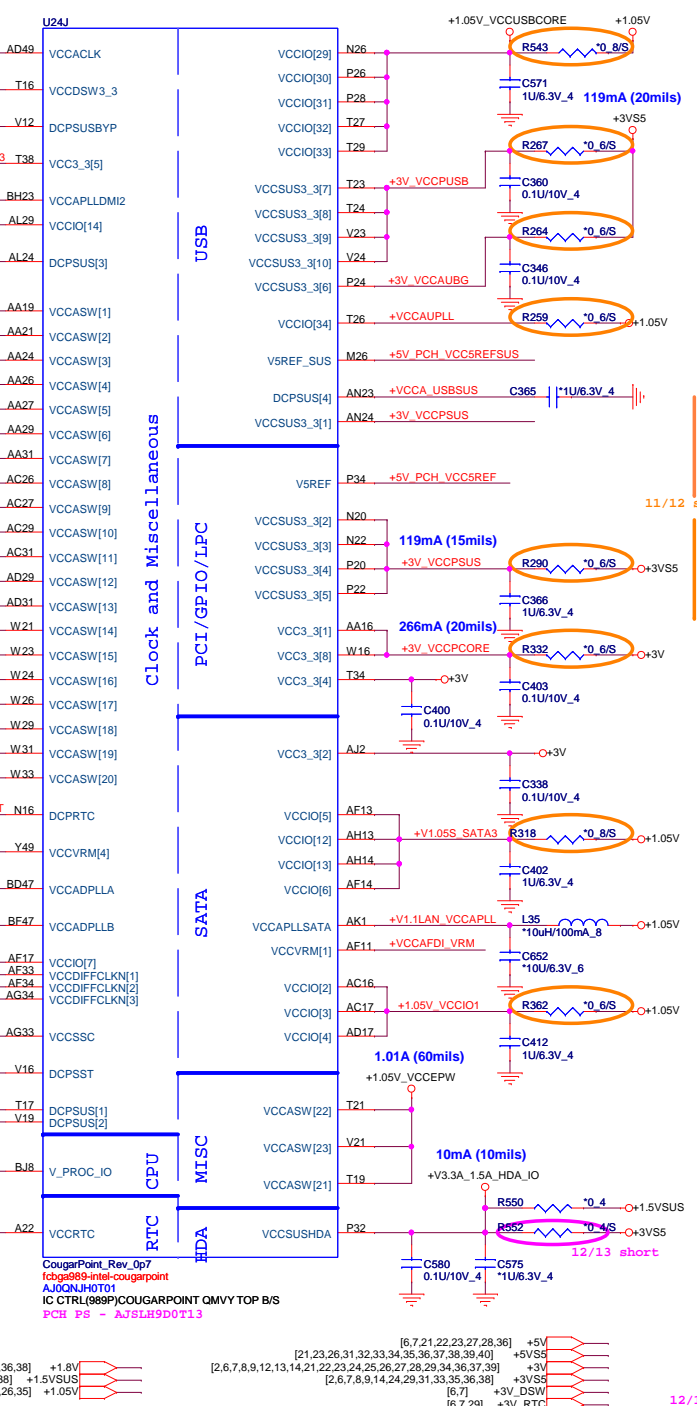
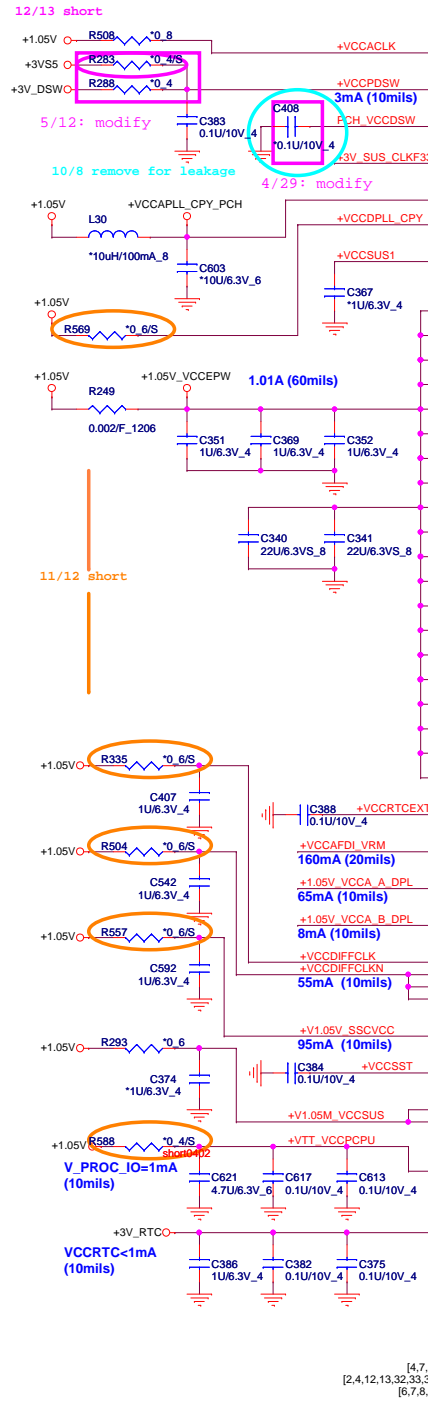


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Cougar Point-M (POWER)



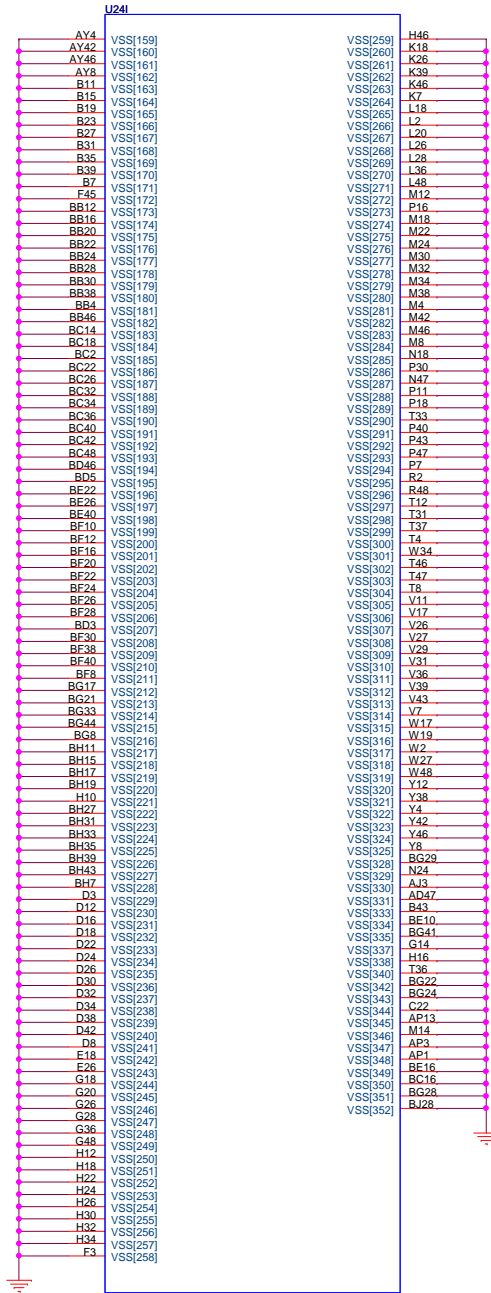
[4,7,36,38]	[6,7,21,22,23,27,28,36]	+5V	
[2,4,12,13,32,33,38]	[21,23,26,31,32,33,34,35,36,37,38,39,40]	+5VSUS	
[6,7,29]	[2,6,7,8,9,12,13,14,21,22,23,24,25,26,27,28,29,34,36,37,39]	+3V	
	[2,6,7,8,9,14,24,29,31,33,35,36,38]	+3VSUS	
	[6,7]	+3V D3W	
	[6,7,29]	+3V_RTC	

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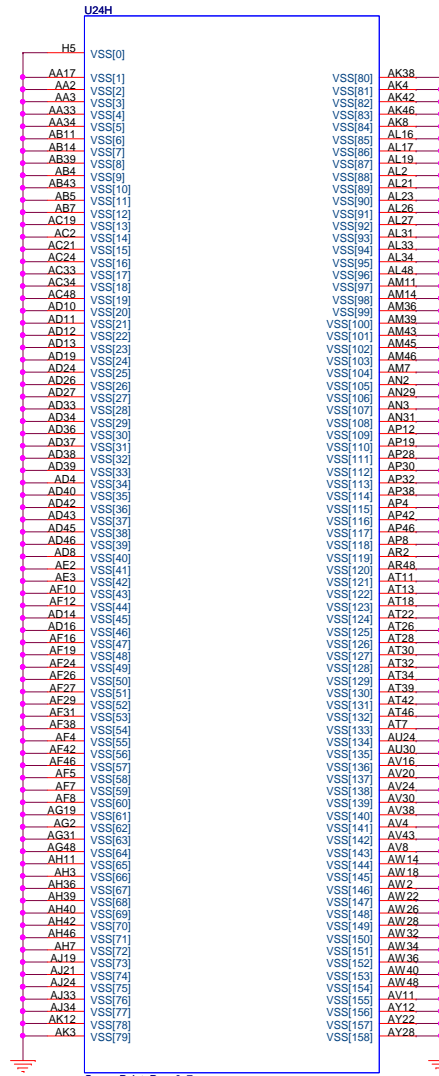
Size Custom	Document Number PCH 5/6 (Power)	Rev A
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IBEX PEAK-M (GND)


IBEX PEAK-M (GND)

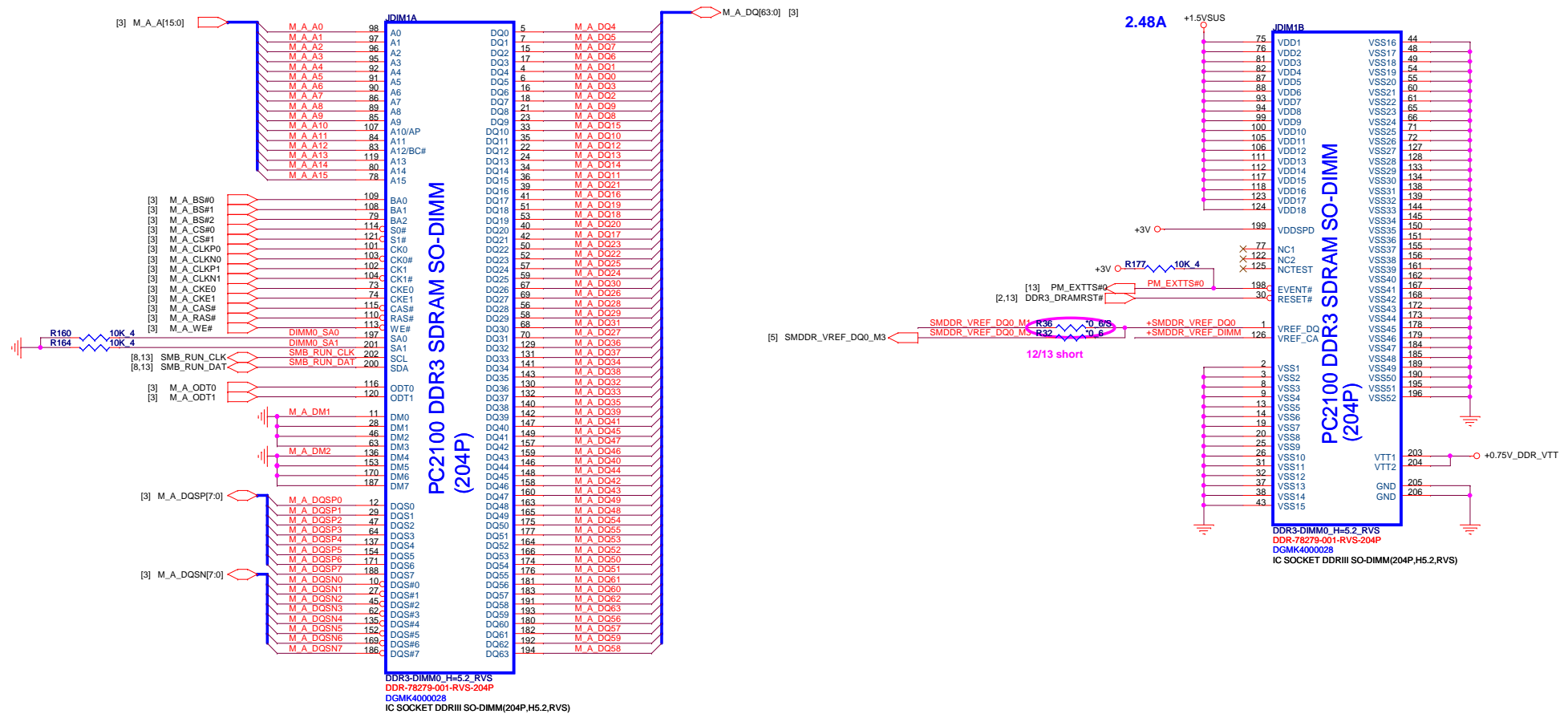


CougarPoint_Rev_0p7
PCH PS - A7SLH9D0T1.3



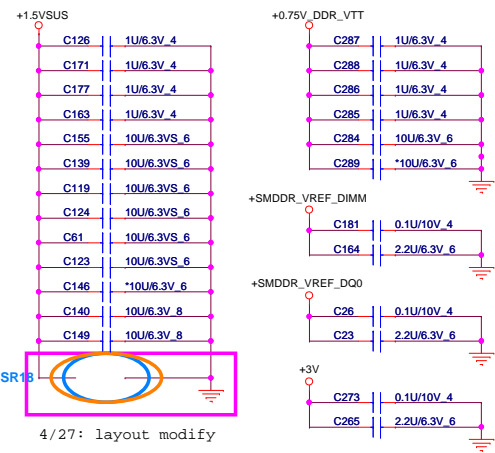
CougarPoint_Rev_0p7
PCH PS - A7SLH9D0T1.3

 NBS	PROJECT : TWH Quanta Computer Inc.		
	Size Custom	Document Number PCH 6/6 (Ground)	Rev A
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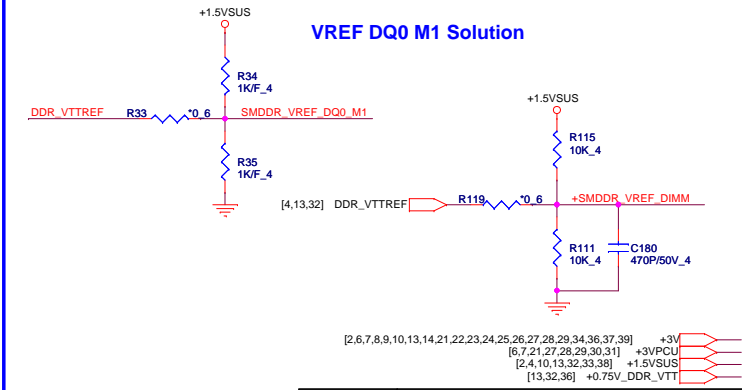


Remove M2 Solution (Intel 436996 Doc)

Place these Caps near So-Dimm0.



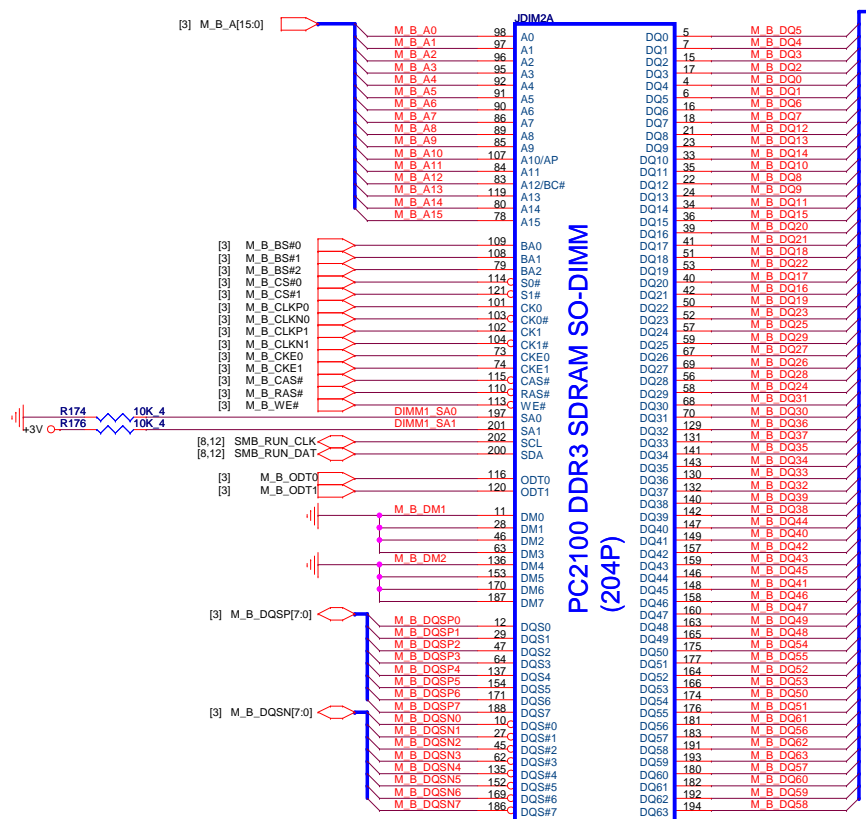
VREF DQ0 M1 Solution



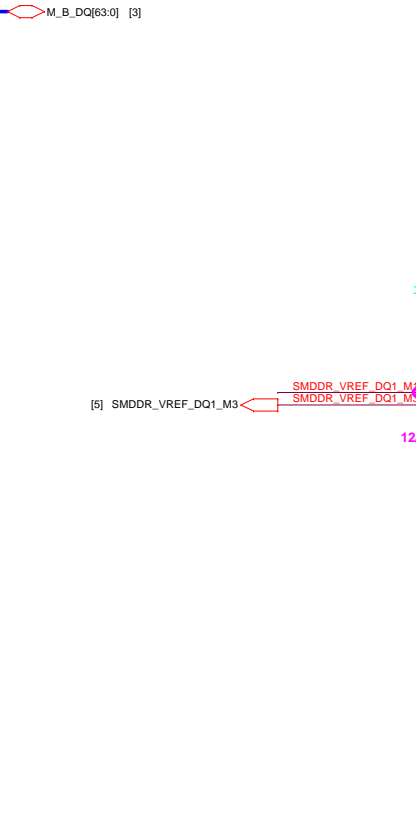
NBS

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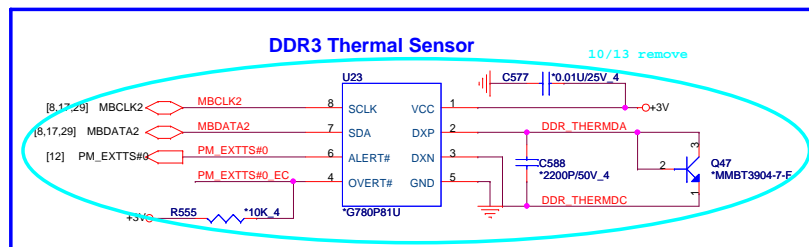
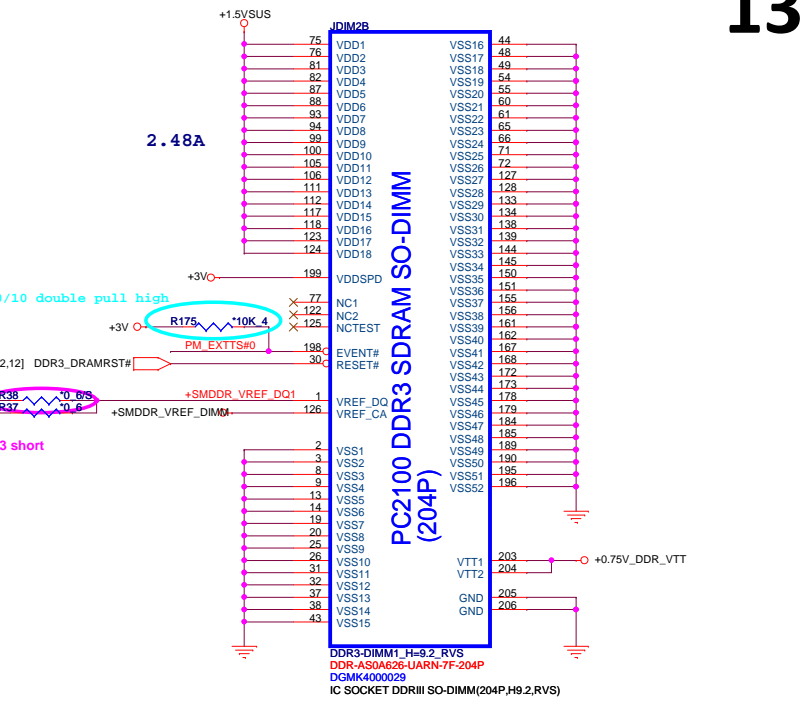
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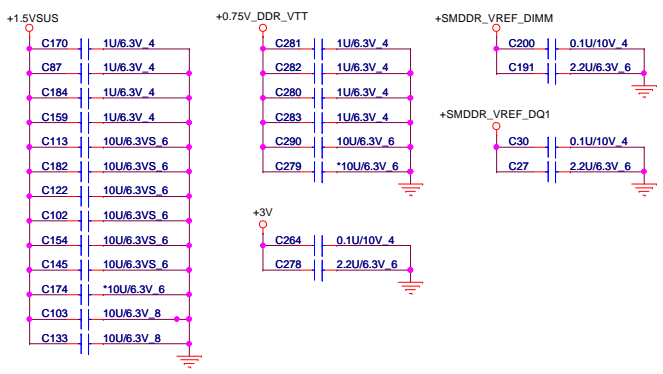
DDR3-DIMM1_H=9.2_RVS
 DDR-AS0A626-UARN-7F-204P
 DGMK4000029
 IC SOCKET DDRIII SO-DIMM(204P,H9.2,RVS)



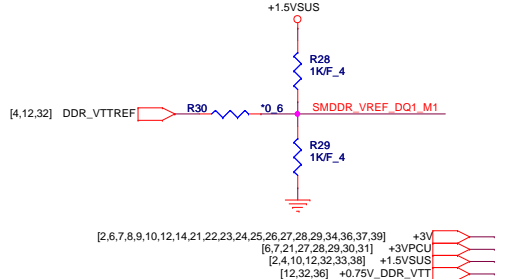
M.B. DQ[63:0] [3]



Remove M2 Solution (Intel 436996 Doc)



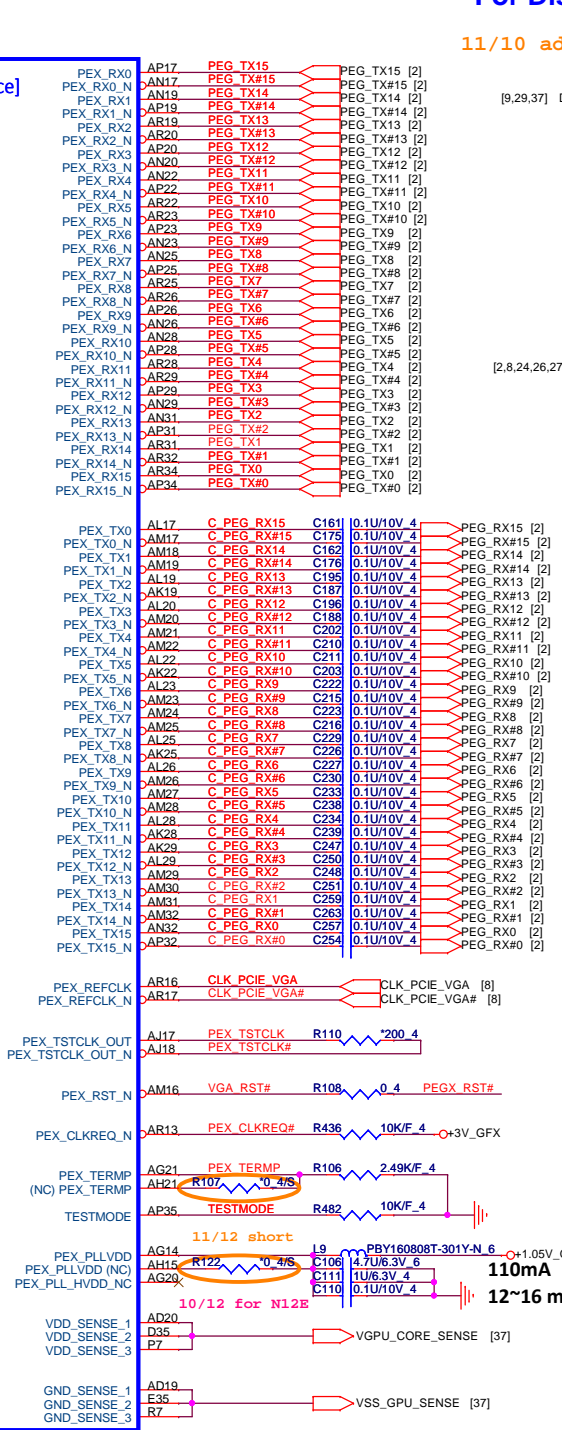
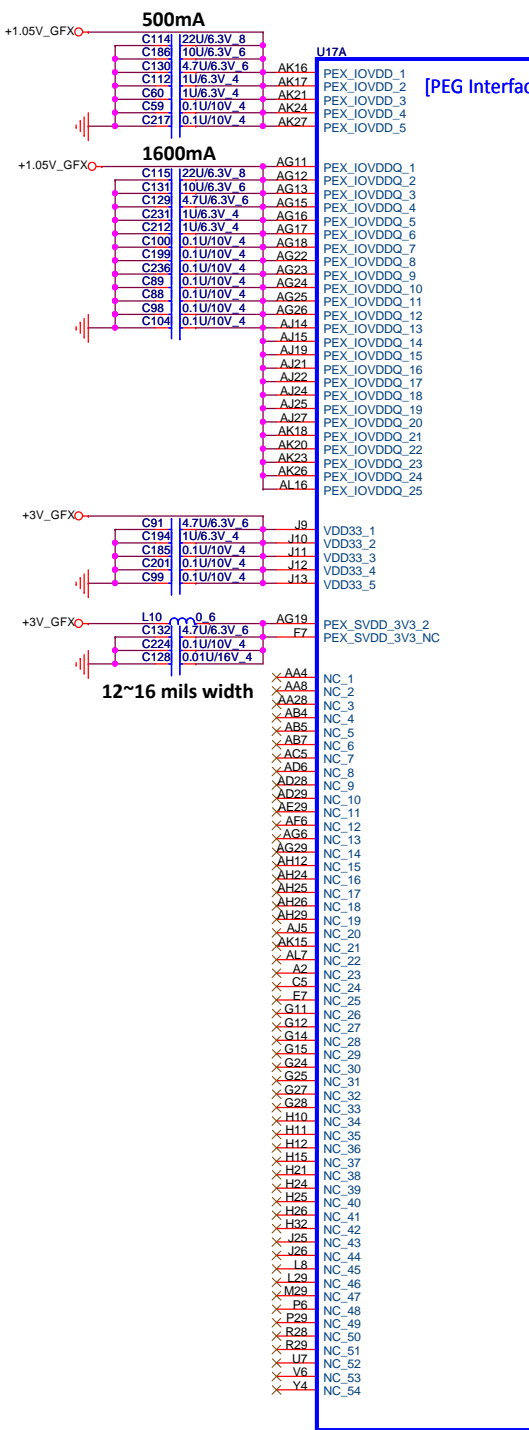
VREF DQ1 M1 Solution



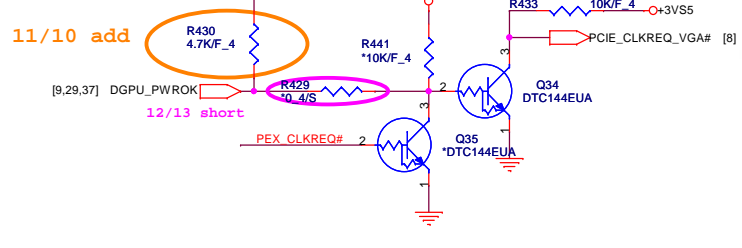
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NBS

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For Discrete



For Discrete

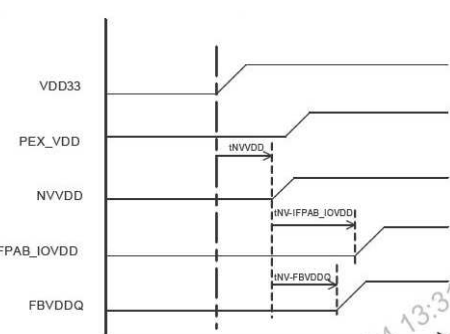
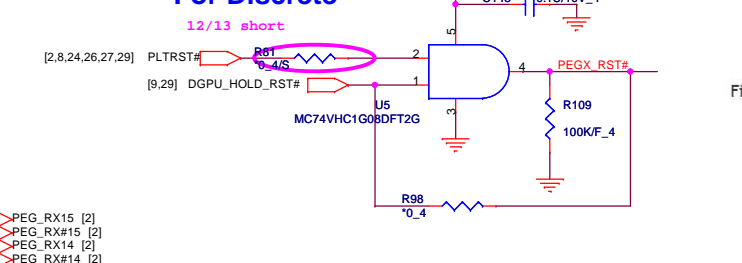


Figure 3.20 Recommended Power On Sequencing Order

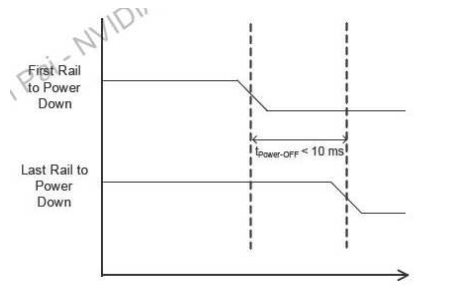


Figure 3.21 Recommended Power Off Sequencing Order

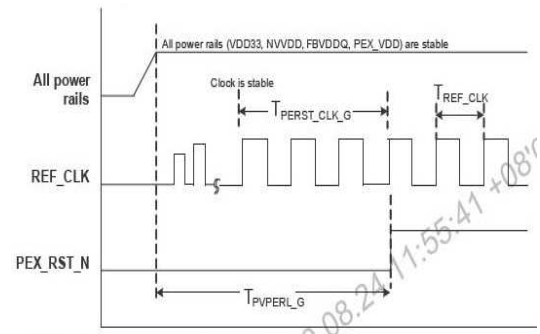


Figure 3-18. PEX_RST_N Timing for GPU

Table 3-8. N11x Reset Requirements for PCI Express 2.0

Constraint Parameter	Requirement	Notes
T_{PVPERL_G}	$T_{PVPERL_G} \geq 1\mu s$	
$T_{PERST_CLK_G}$	$T_{PERST_CLK_G} \geq 11T_{REF_CLK}$	

NVVDD Settling Time

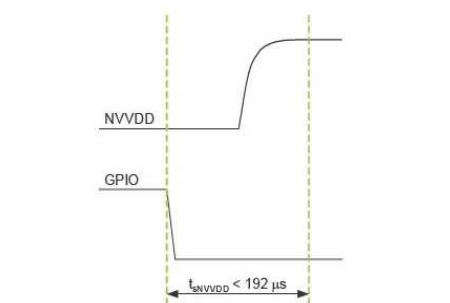
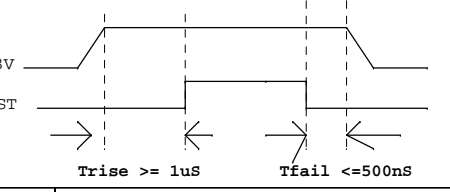


Figure 3.12 NVVDD Settling Time

PEX_RST timing

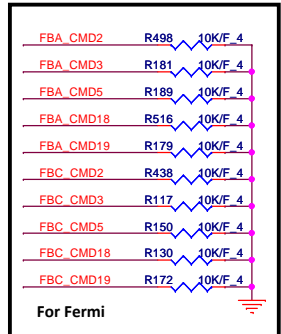
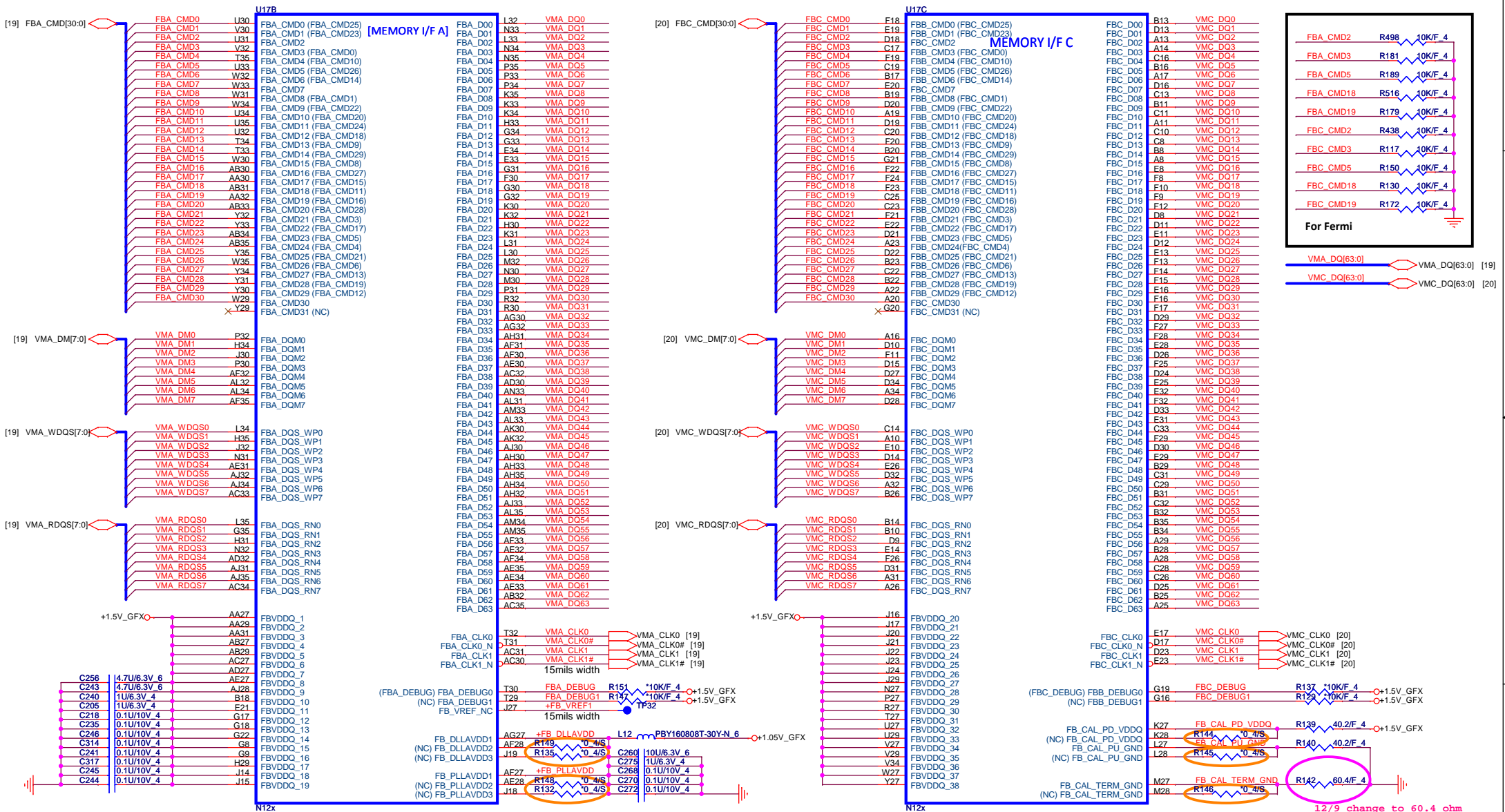


N12P AJON12P0T04

[15,16,37,38] +1.05V_GFX
[16,17,22,37,38] +3V_GFX

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N12x N12P AJ0N12P0T04

10/12 for N12E 11/12 short

N12x N12P AJ0N12P0T04

10/12 for N12E 11/12 short

12/9 change to 60.4 ohm

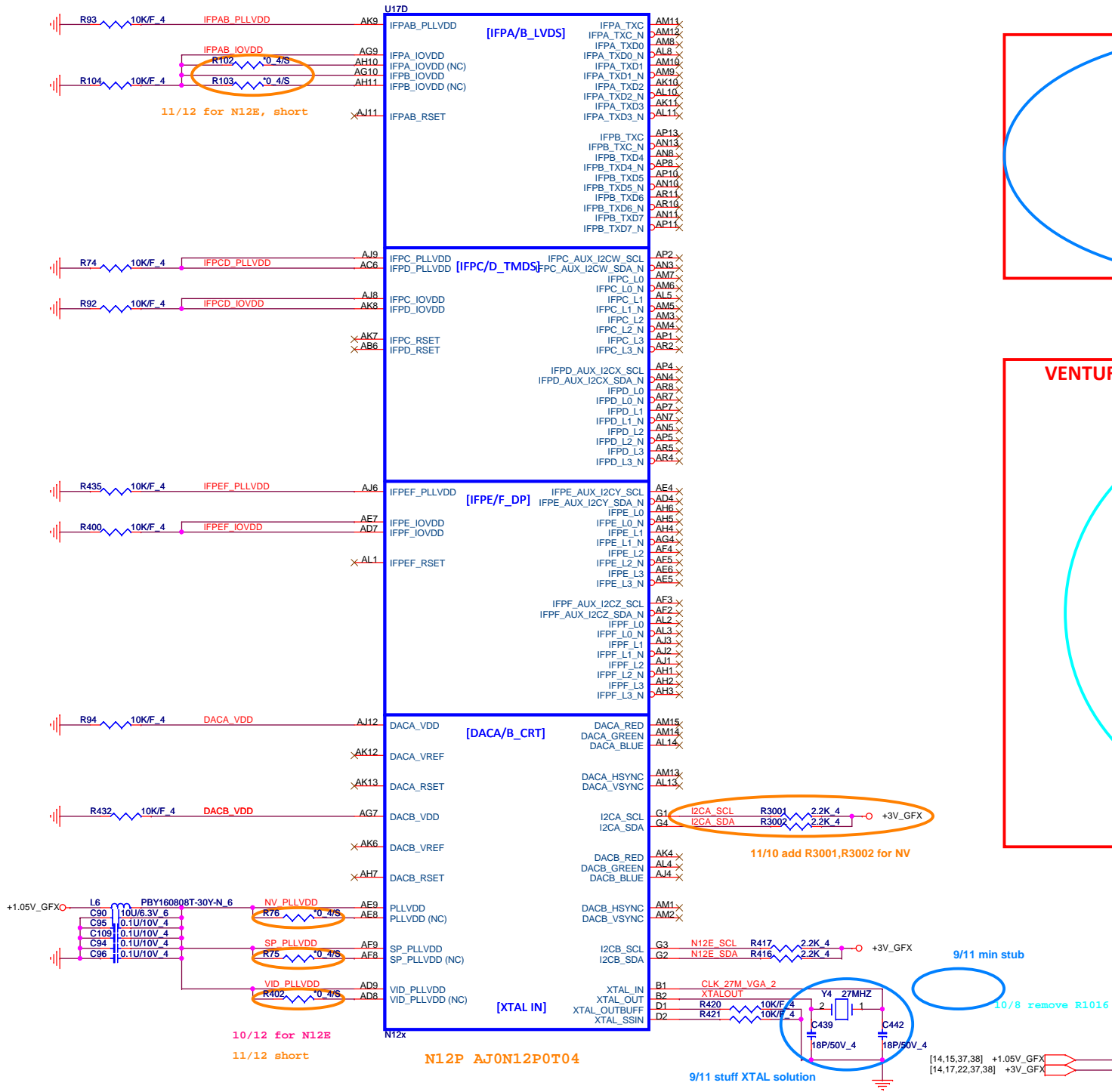
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[14,16,37,38] +1.05V_GFX
 [19,20,37,38] +1.5V_GFX



10/8 remove 27M clock buffer circuit

VENTURA Function(N12E Only)

9/28
Nvidia announce - N12E no support Ventura
N12E only support Dual Core CPU (35W)

10/7
remove all ventura circuit

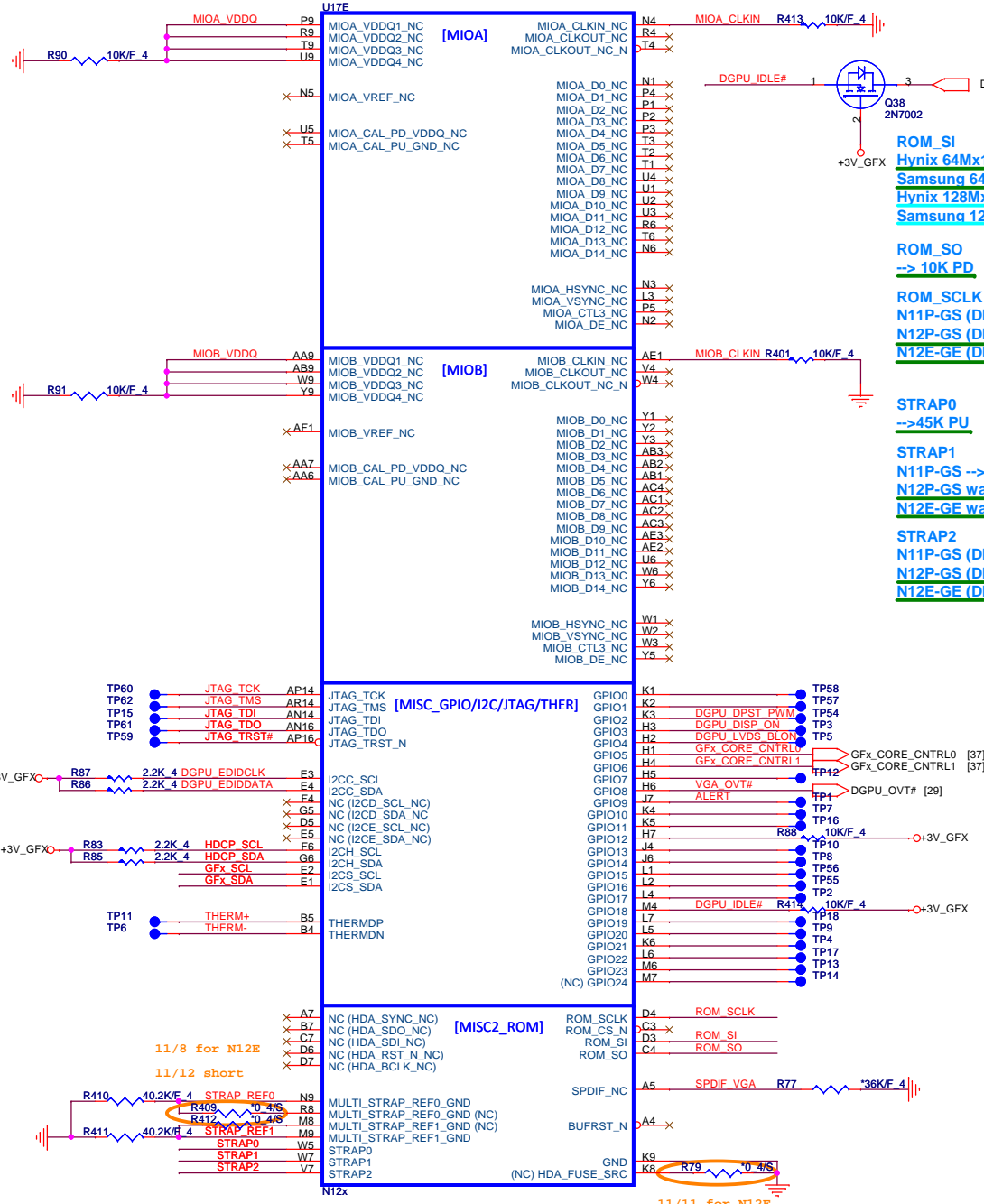


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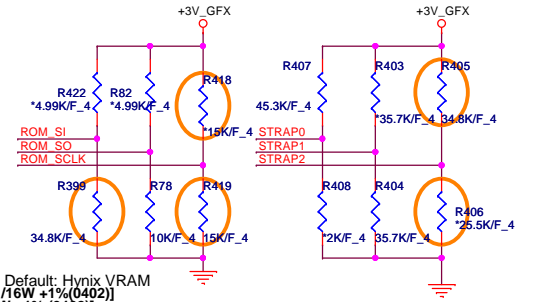
N11P-GS ES
Strap2 = 35K Pull High
ROM_CLK=15k Pull High

N11P-GS QS
Strap2 = 5K Pull High
ROM_CLK=15k Pull High



Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111



ROM_SI
Hynix 64Mx16 -->15K PD
Samsung 64Mx16 -->20K PD
Hynix 128Mx16 -->35K PD
Samsung 128Mx16 -->45K PD

ROM_SO
--> 10K PD

ROM_SCLK
N11P-GS (DID=0DF0) ----> 15k PU
N12P-GS (DID=0DF4) ---->15K PU
N12E-GE (DID=0DCE) ---->15K PU

STRAP0
-->45K PU

STRAP1
N11P-GS -->35K PD
N12P-GS waiting PUN update
N12E-GE waiting PUN update

STRAP2
N11P-GS (DID=0DF0) ----> 5k PD
N12P-GS (DID=0DF4) ---->25K PD
N12E-GE (DID=0DCE)---->35K PU

Default: Hynix VRAM
4.99K/F 4: CS24992FB26 [RES CHIP 4.99K 1/16W +1%(0402)]
10K/F 4: CS31002FB26 [RES CHIP 10K 1/16W +1% (0402)]
15K/F 4: CS31502FB24 [RES CHIP 15K 1/16W +1% (0402)]
20K/F 4: CS32002FB29 [RES CHIP 20K 1/16W +1%(0402)]
30.1K/F 4: CS33012FB18 [RES CHIP 30.1K 1/16W +1%(0402)]
35.7K/F 4: CS33572FB13 [RES CHIP 35.7K 1/16W +1%(0402)]
45.3K/F 4: CS34532FB18 [RES CHIP 45.3K 1/16W +1%(0402)]

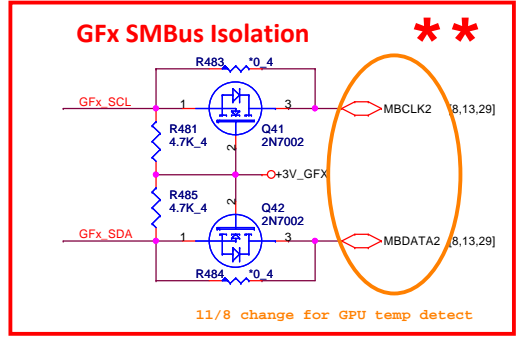
	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0		
ROM_SO	NB10X	XCLK_417	FB_O_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK		PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	0010
ROM_SI		RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2		PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	1000
STRAP1		3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0001
STRAP0		USER[3]	USER[2]	USER[1]	USER[0]	1111

VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI
0000		Reserved		
0001	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Qimonda	IDGH1G-04A1F1C-16X	PD 10K
0010	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Hynix	H5TQ1G63BFR-12C	PD 15K
0011	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Samsung	K4W1G1646E-HC12	PD 20K
0110		Reserved		
XXXX	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Hynix	H5TQ1G63AFR-14C	
XXXX	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Samsung	K4W1G1646D-EC12	

GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVDD VID0
6	OUT	N/A	NVDD VID1
7	OUT	N/A	NVDD VID2 ^{11/13}
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL ^{11/13}
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL

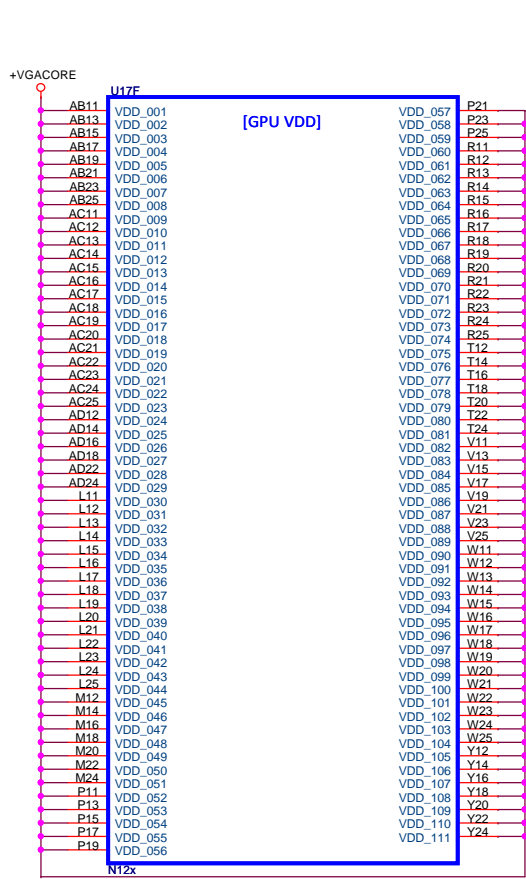


N12P AJ0N12P0T04

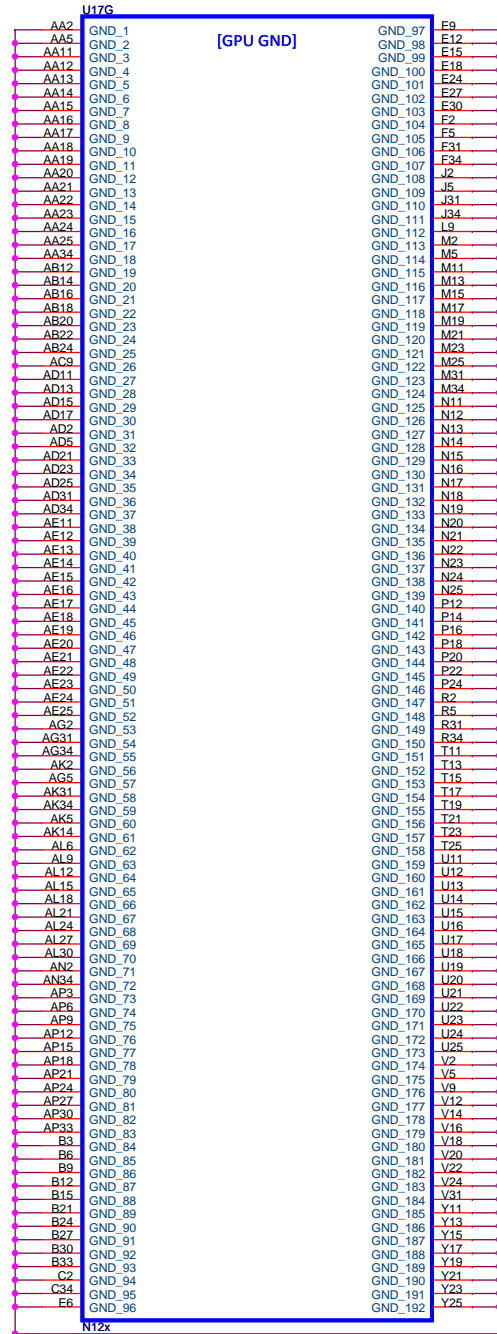
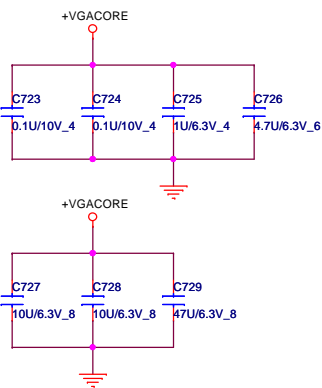
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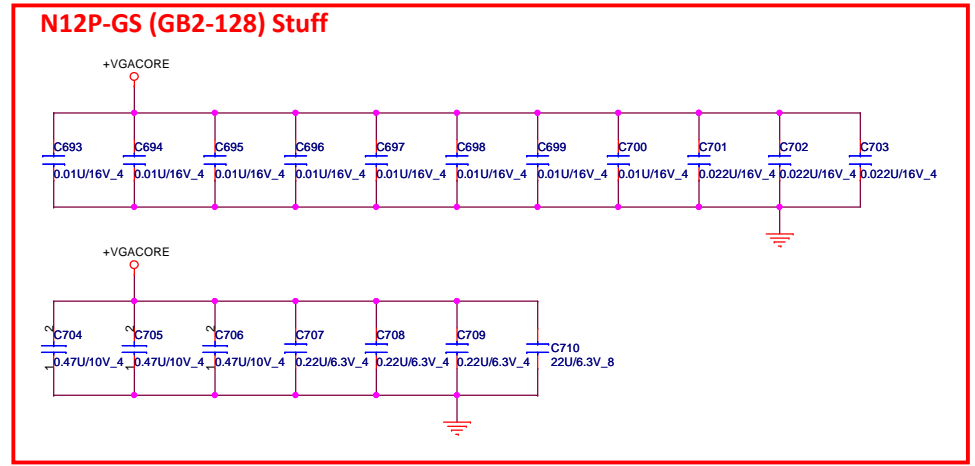
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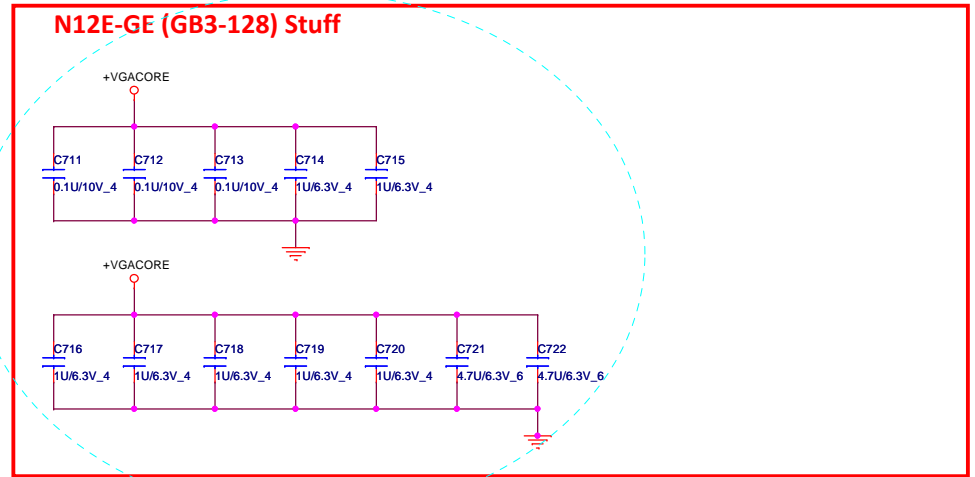
N12P AJON12P0T04



N12P AJON12P0T04



N12E-GE: C395, C396, C397, C398, C399, C400, C401, C402, C403, C404, C405, C406, C407, C408, C409, C410, C411 stuff 0.1U/10V_4. N12E-GE: C412 Stuff 47U/6.3V_8

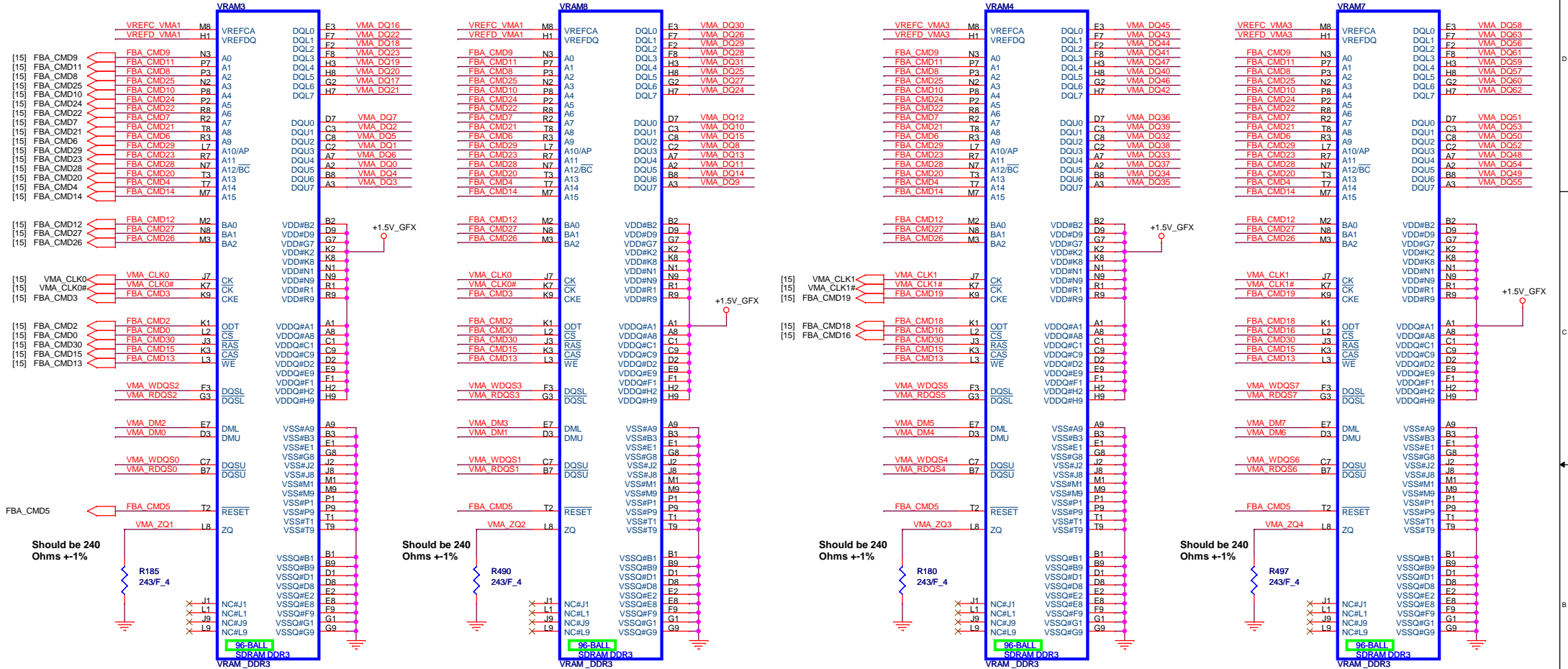


9/28 need check for N12E

[37] +VGACORE

		PROJECT : TWH Quanta Computer Inc.	
		Size A3 Date: Tuesday, January 04, 2011	Document Number DGPU 5/5 (Power/Ground)

CHANNEL A: 256MB/512MB DDR3

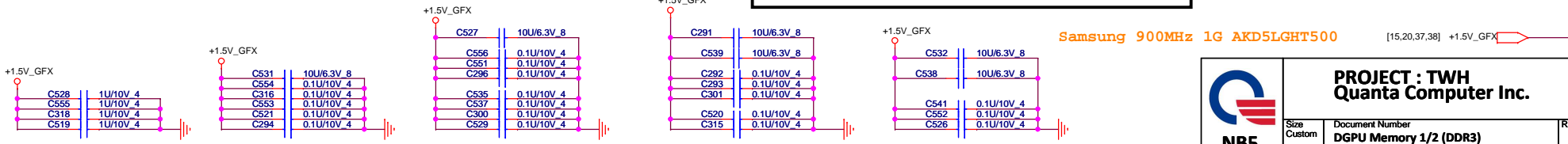


VMA_CLK0
 R178
 160/F_4
 VMA_CLK0#

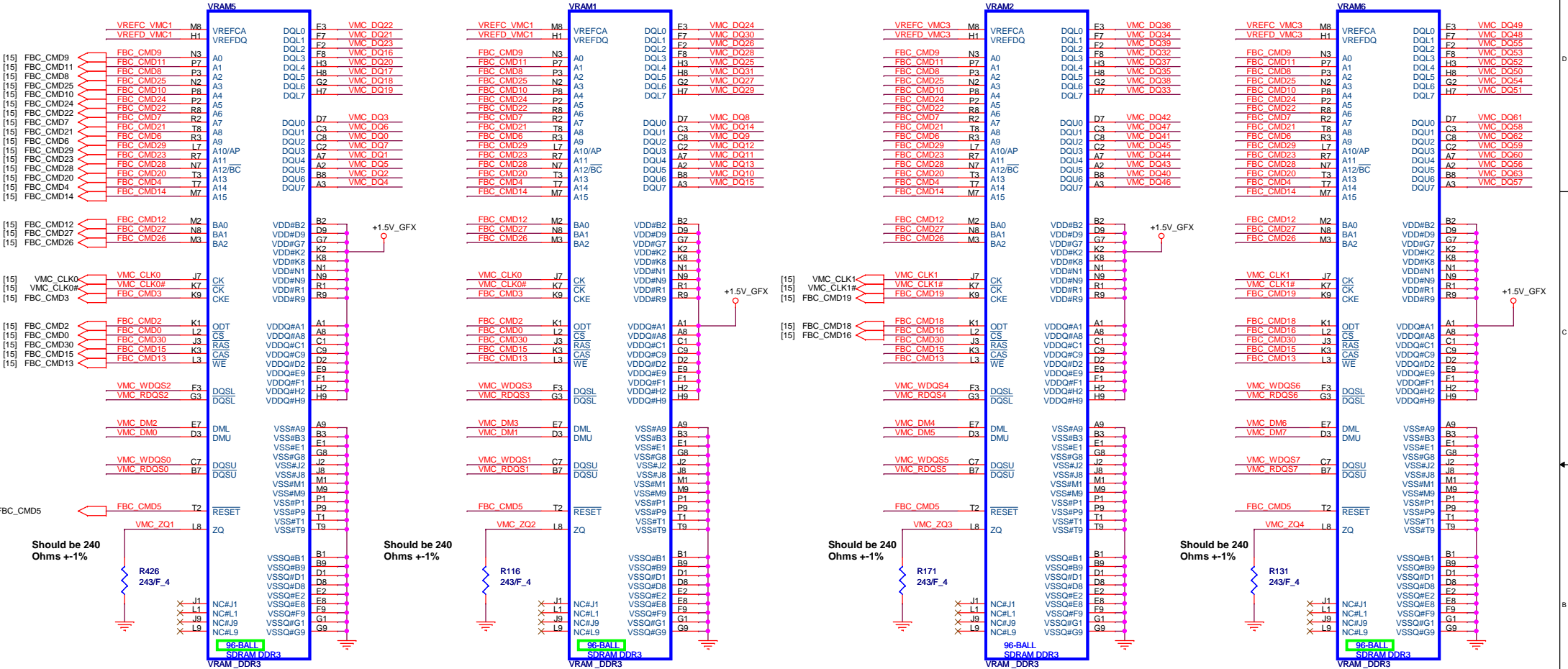
Fermi : Change to 160 ohm
 1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
 2 : CS11622PB07 ,RES CHIP 162 1/16W +-1%(0402)

VMA_CLK1#
 R183
 160/F_4
 VMA_CLK1#

Fermi : Change to 160 ohm
 1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
 2 : CS11622PB07 ,RES CHIP 162 1/16W +-1%(0402)



CHANNEL B: 256MB/512MB DDR3

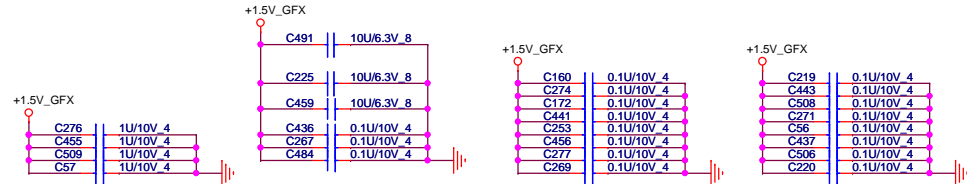


Should be 240 Ohms +-1%

VMC CLK0
 R61 160F_4
 VMC CLK0#
 Fermi : Change to 160 ohm
 1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
 2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

Should be 240 Ohms +-1%

VMC CLK1
 R173 160F_4
 VMC CLK1#
 Fermi : Change to 160 ohm
 1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
 2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

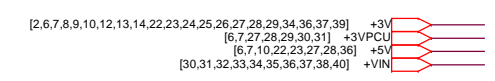
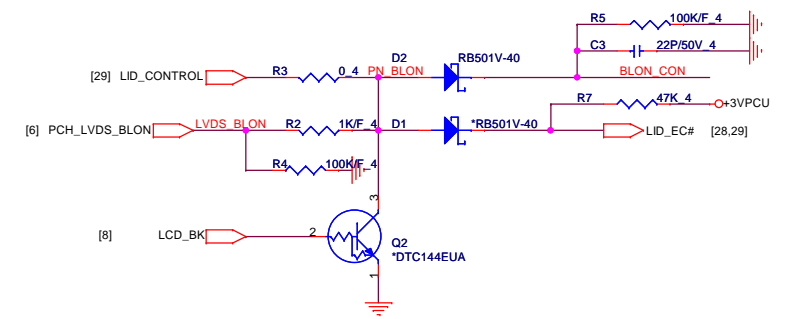
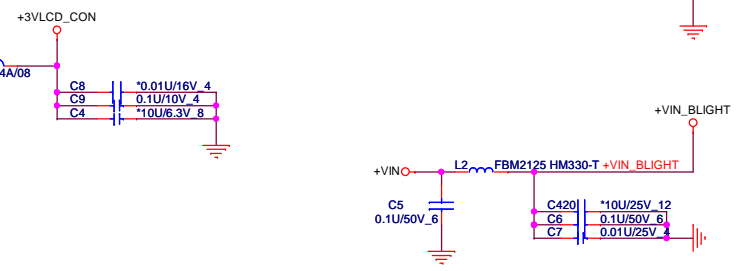
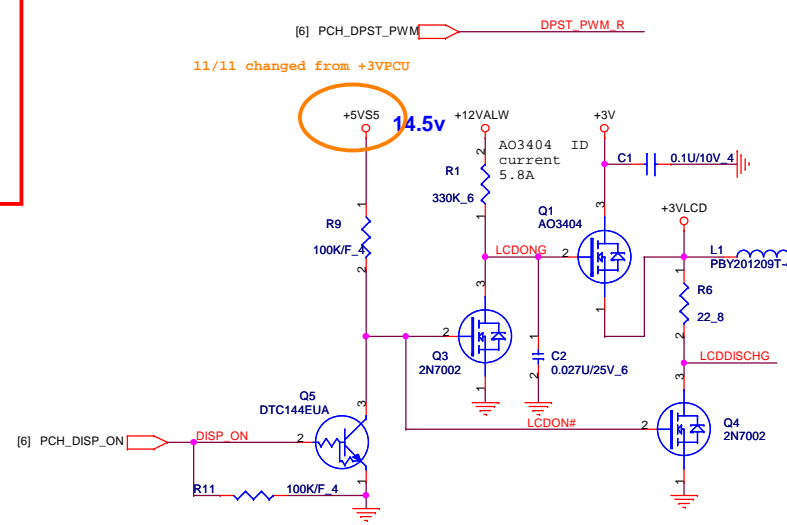
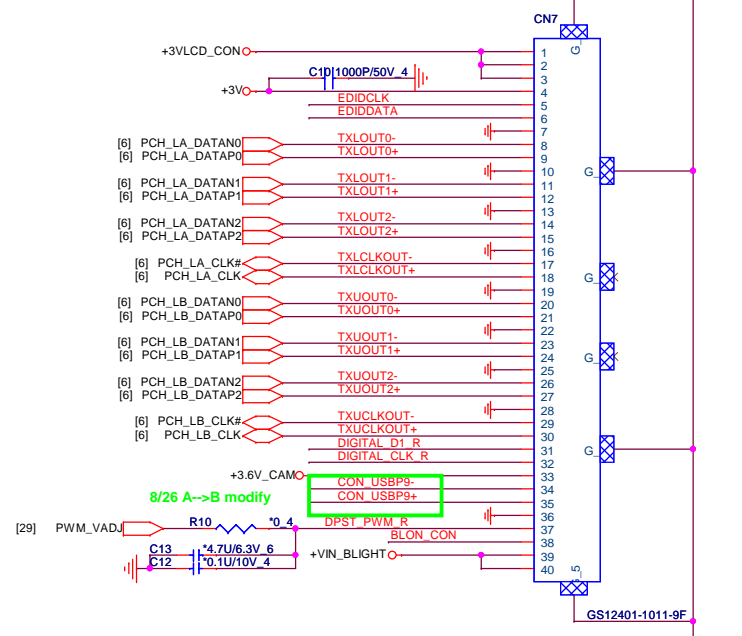
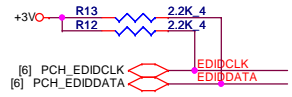
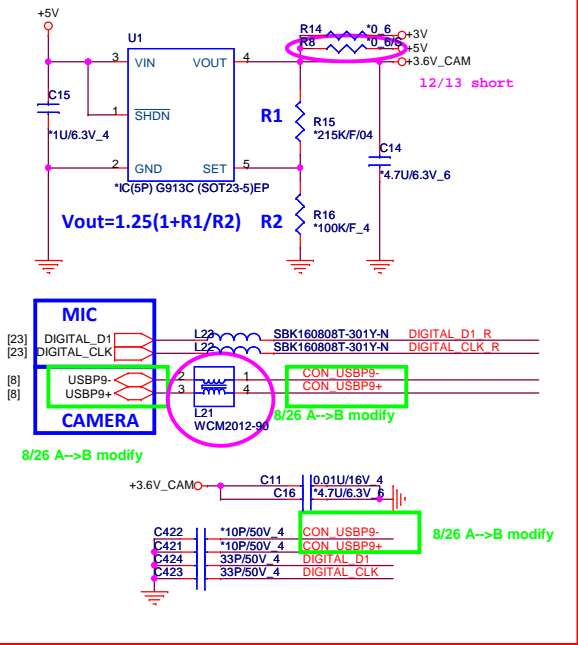


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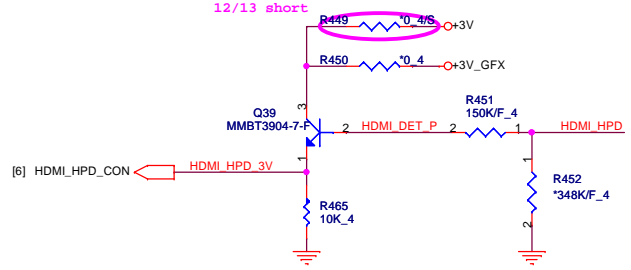
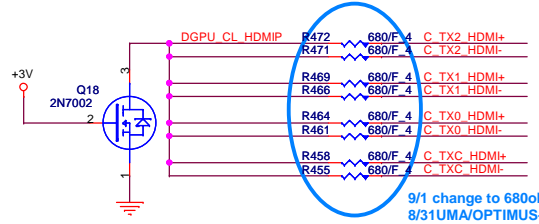
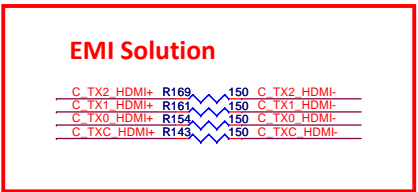
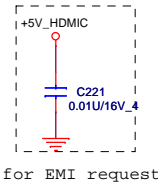
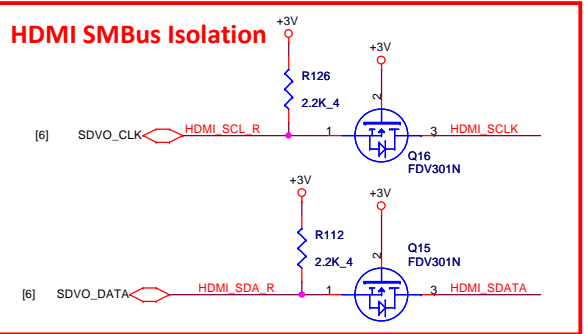
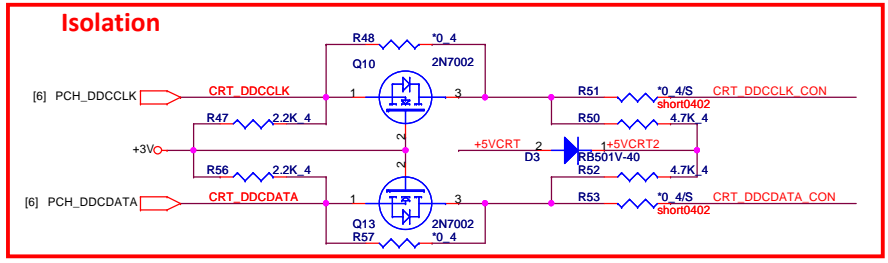
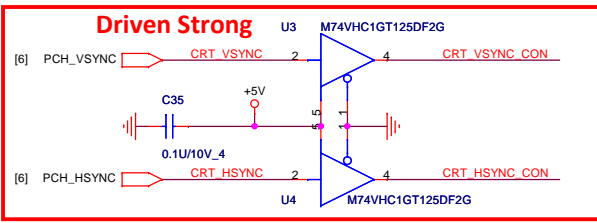
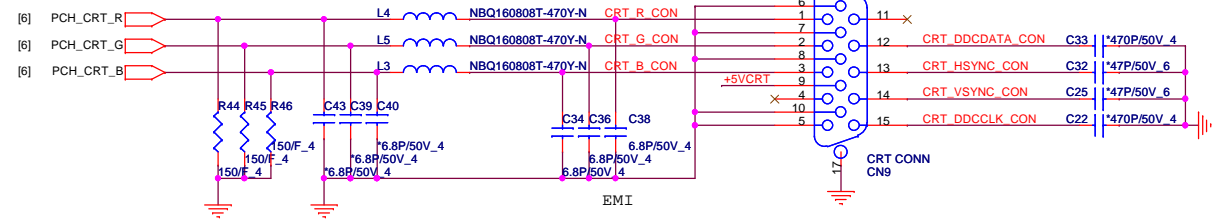
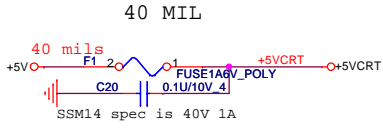
Samsung 900MHz 1G AKD5LGH500

USB Camera Connector

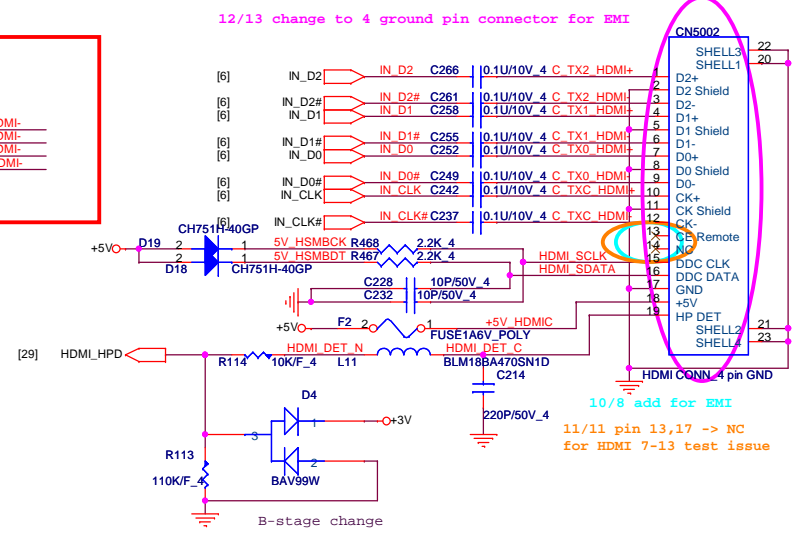


	PROJECT : TWH Quanta Computer Inc.		Rev A
	Size Custom	Document Number LCD Connector (LVDS)	
Date: Tuesday, January 04, 2011		Sheet 21 of 40	

CRT PORT



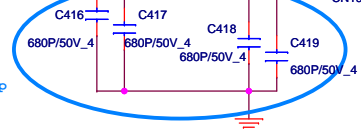
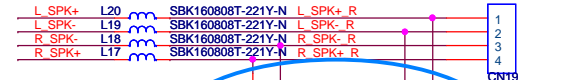
HDMI PORT



PROJECT : TWH
Quanta Computer Inc.

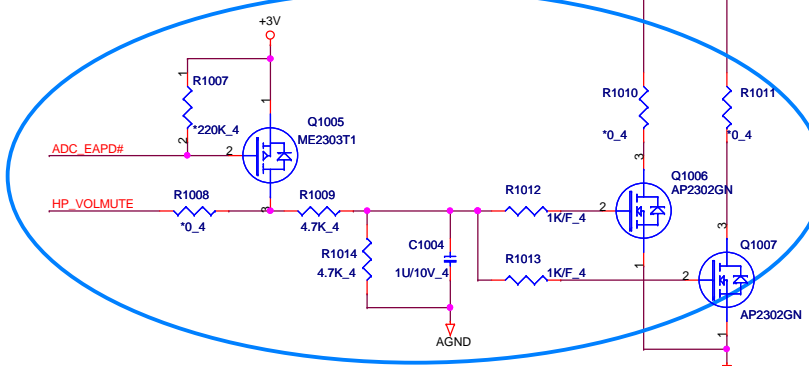
Size Custom	Document Number CRT/HDMI Connector	Rev A
Date: Tuesday, January 04, 2011 Sheet 22 of 40		

Internal Speaker

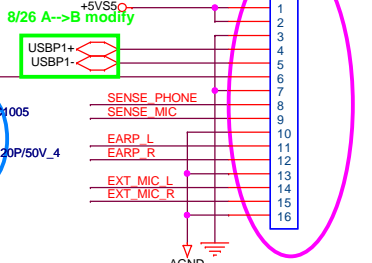


9/8 EMI need change to 680p

9/5 add de-pop circuit, add C1002, C1003, C1004 Q1005, Q1006, Q1007 R1007, R1008, R1009, R1010, R1011, R1012, R1013, R1014

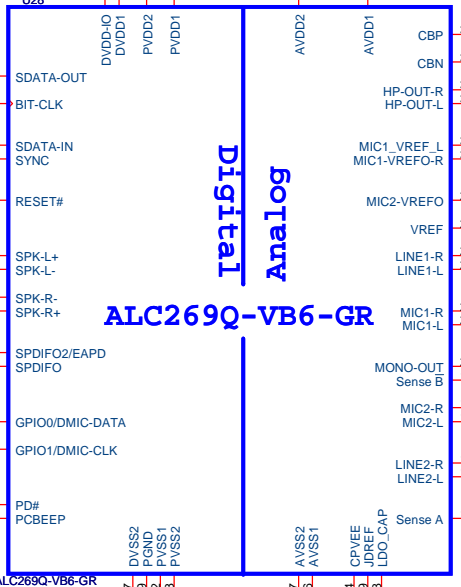


12/8 change to 16 pin connector (add 2 AGND pin)



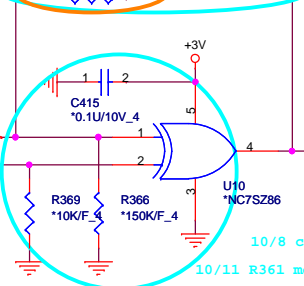
8/26 A->B modify

9/8 EMI (near CN18)



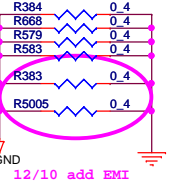
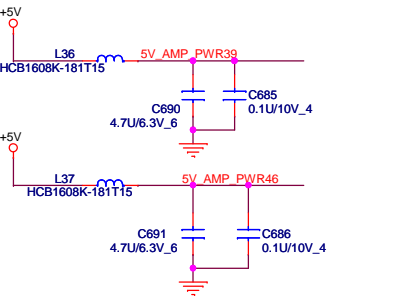
10/5 change VB6

11/12 short
 R361 0.4/S HDA BEEP1



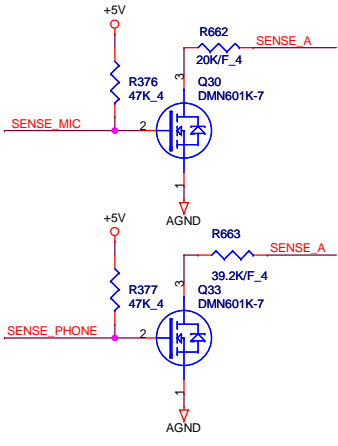
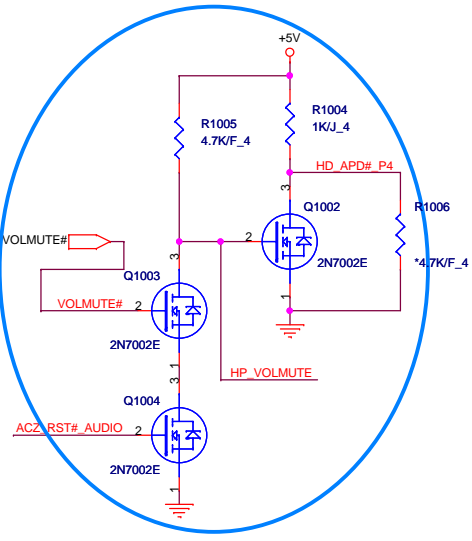
10/8 change net name

10/11 R361 mount, other unmount



12/10 add EMI

9/5 "PD#" circuit modify
 1.delete R650, R372, R373, Q27, Q28, D16, D17, D15
 2.add Q1002, Q1003, Q1004, R1004, R1005, R1006



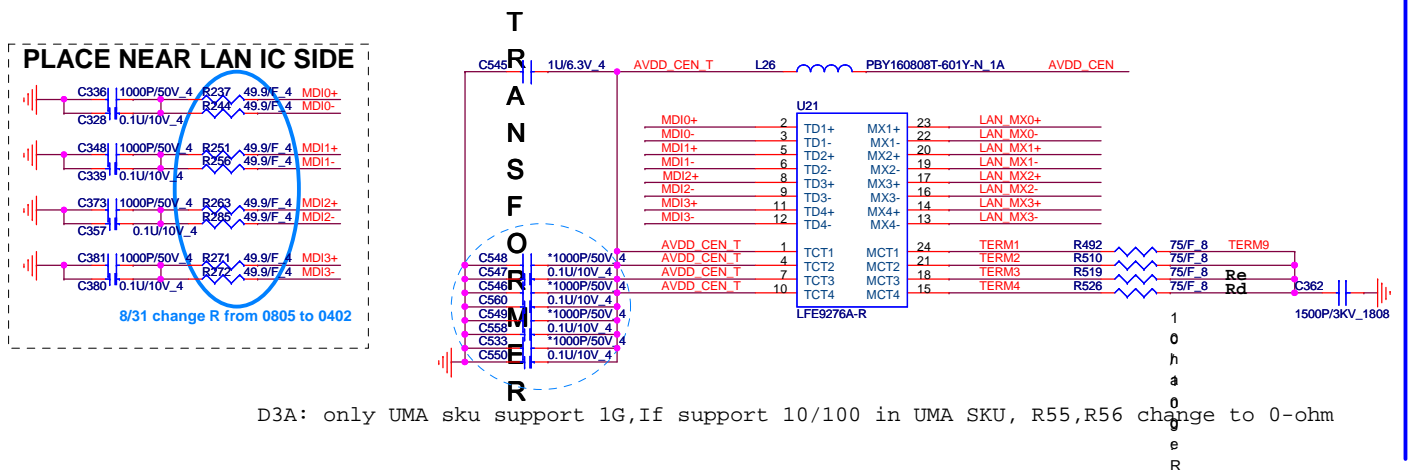
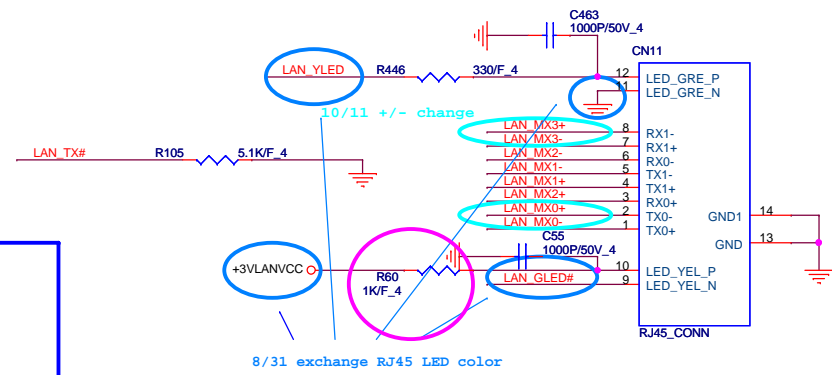
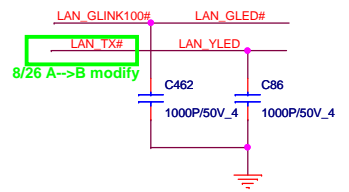
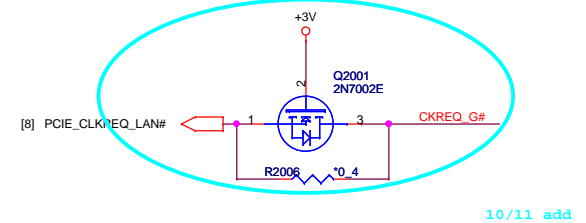
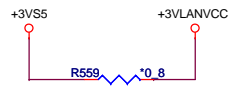
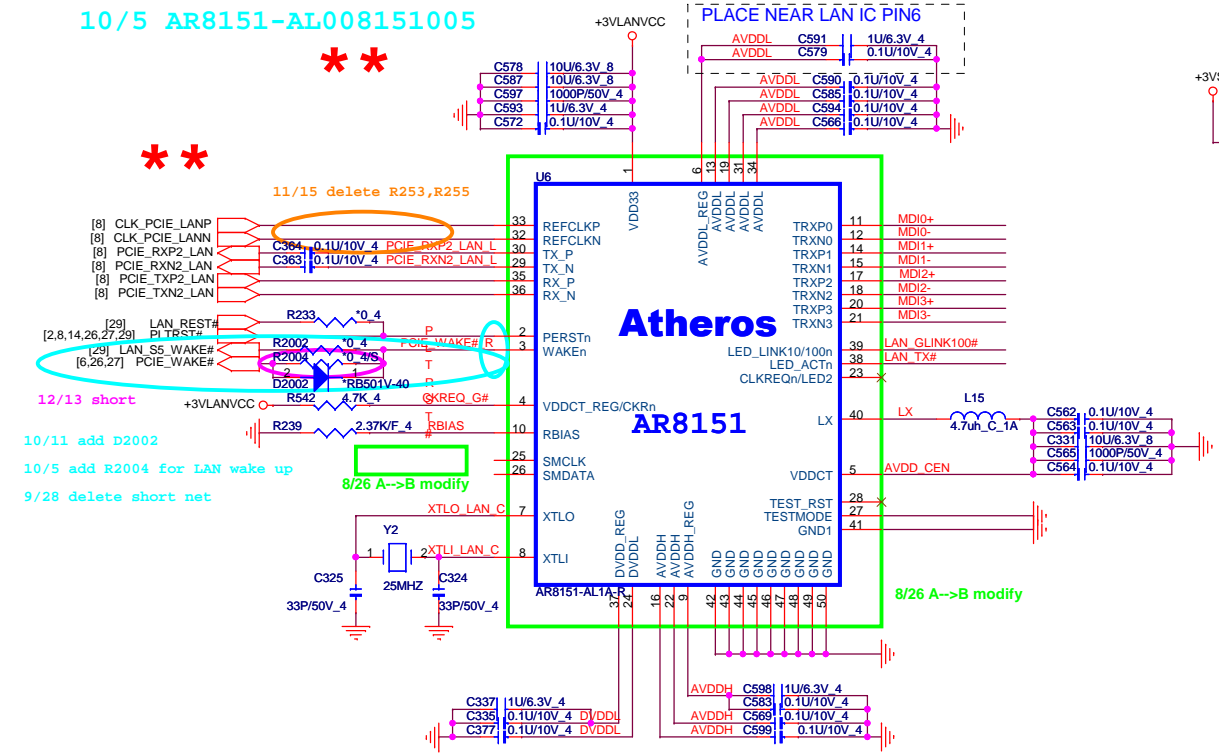
PROJECT : TWH
Quanta Computer Inc.

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Atheros Lan

10/5 AR8151-AL008151005



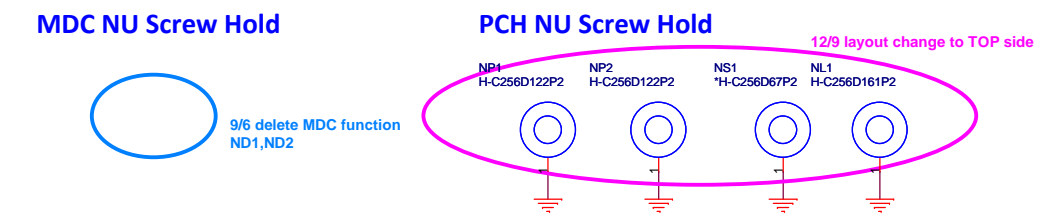
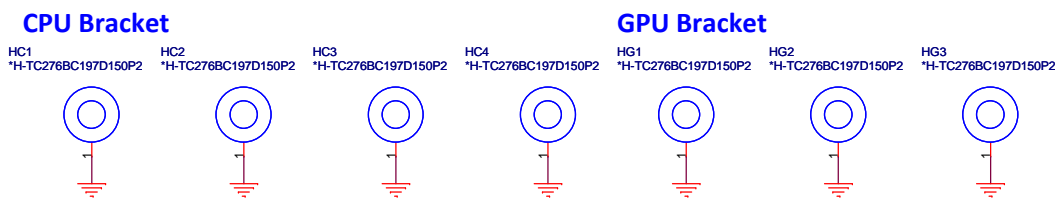
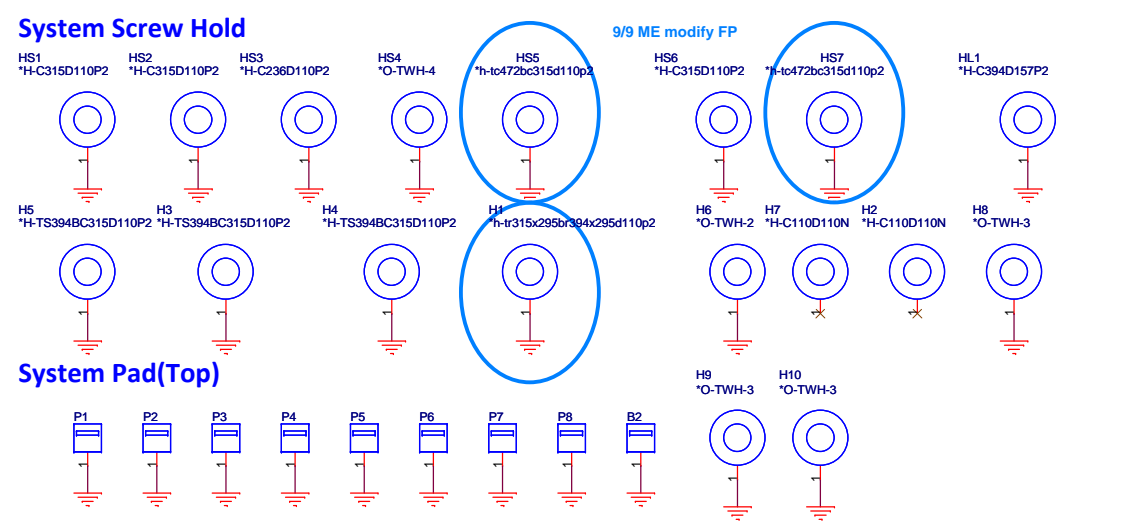
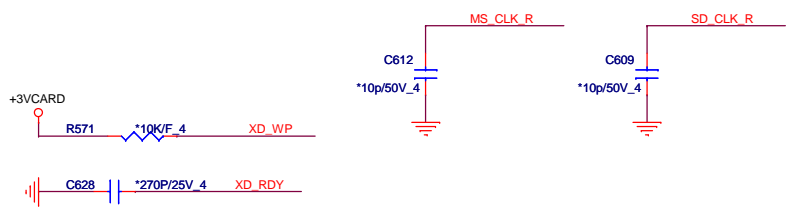
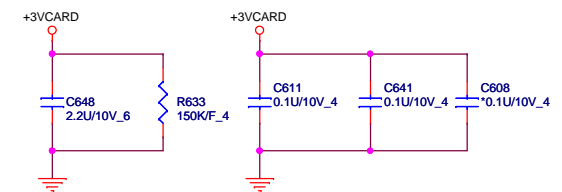
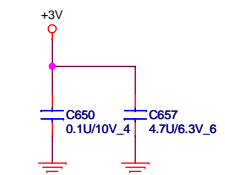
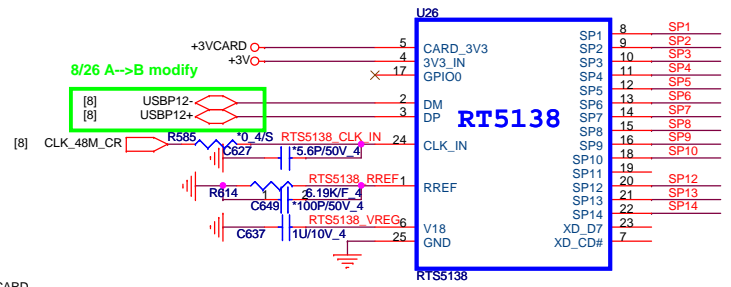
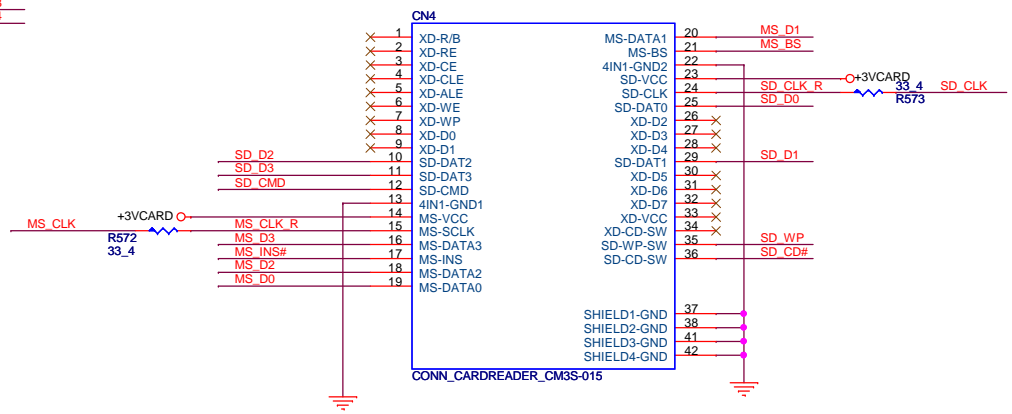
D3A: only UMA sku support 1G, If support 10/100 in UMA SKU, R55, R56 change to 0-ohm

PROJECT : TWH
Quanta Computer Inc.

Size Custom	Document Number LAN Controller (Atheros_AR8151)	Rev A
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SP1	XD_RDY	SD_WP	MS_CLK
SP2	XD_RE#		MS_INS#
SP3	XD_CE#	SD_D1	
SP4	XD_CLE	SD_D0	
SP5	XD_ALE	SD_D7	MS_D3
SP6	XD_WE#	SD_CMD#	
SP7	XD_WP	SD_D6	
SP8	XD_D0	SD_CLK	MS_D2
SP9	XD_D1	SD_D5	MS_D0
SP10	XD_D2	SD_CMD	
SP12	XD_D4	SD_D3	MS_D1
SP13	XD_D5	SD_D2	
SP14	XD_D6		MS_BS

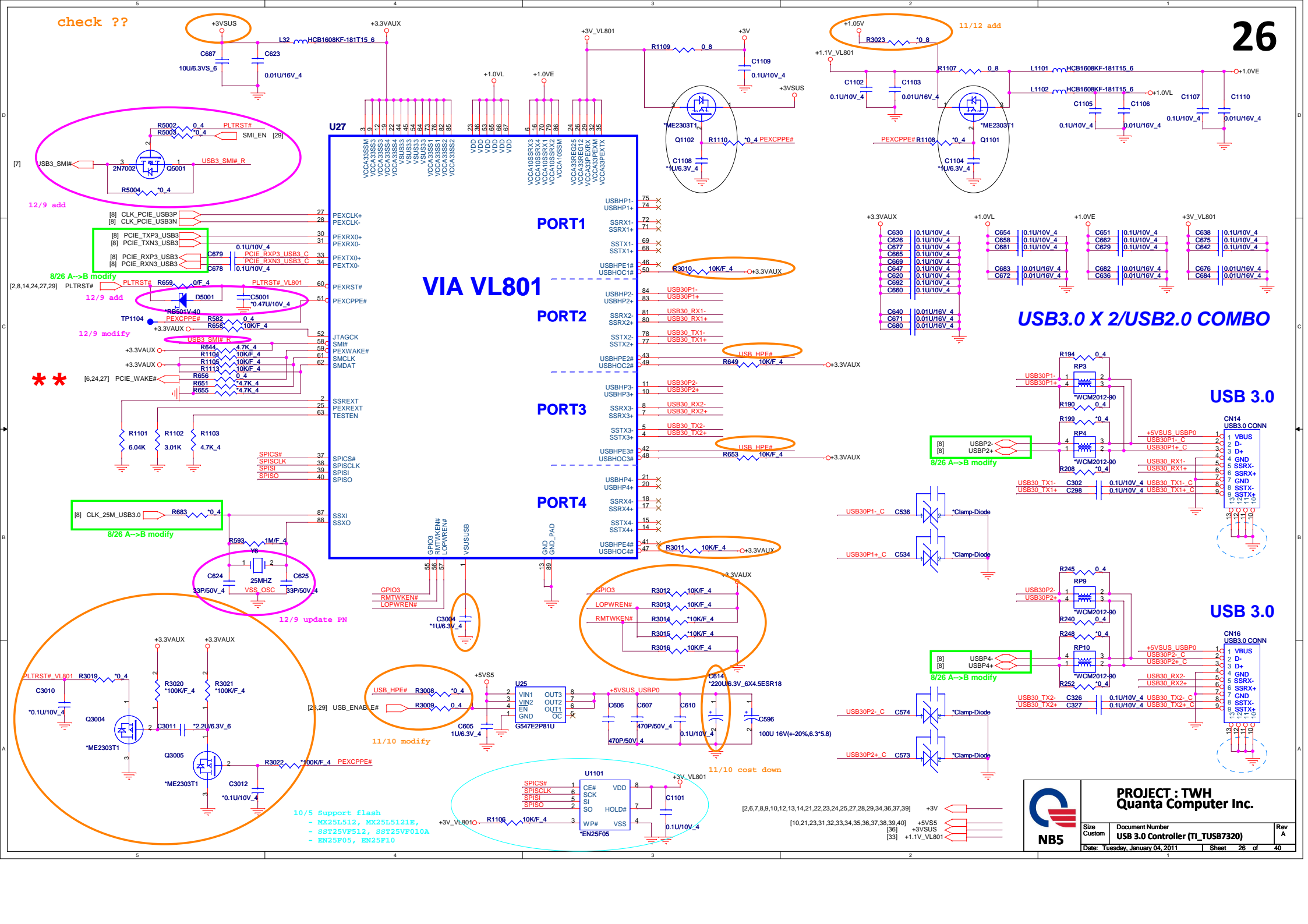
Share Pin



PROJECT : TWH
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check ??



VIA VL801

PORT1

PORT2

PORT3

PORT4

USB3.0 X 2/USB2.0 COMBO

USB 3.0

USB 3.0

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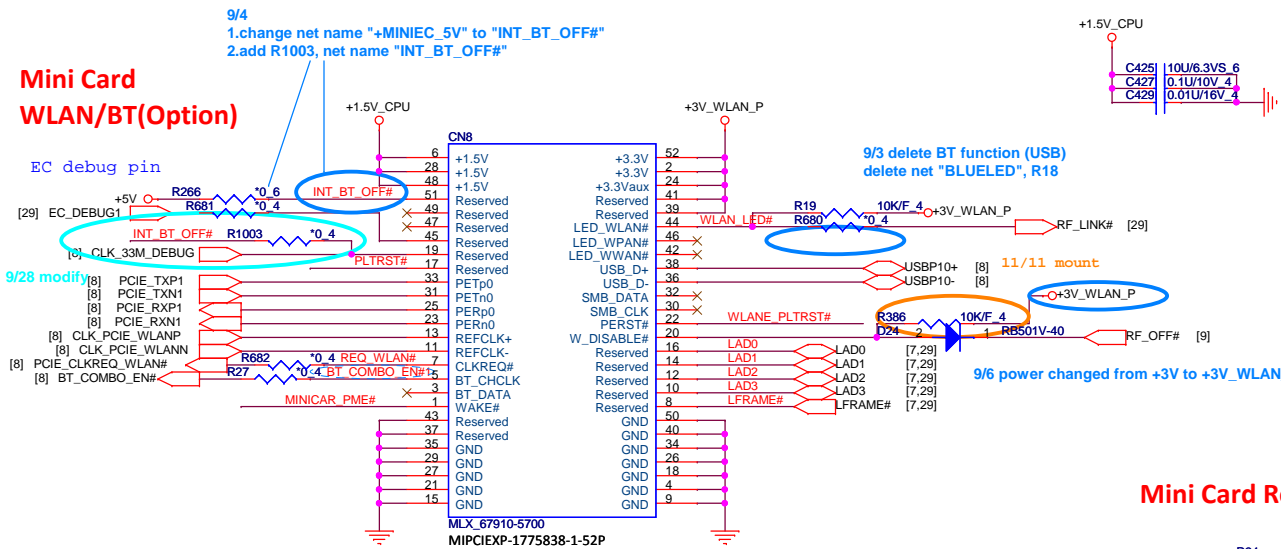


Size Custom	Document Number USB 3.0 Controller (T1_TUSB7320)	Rev A
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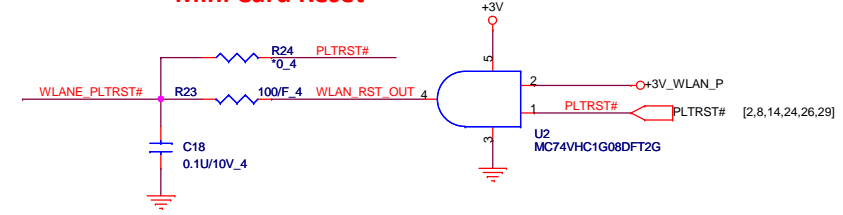
- 21/5 Support flash
 - MX25L512, MX25L512E,
 - SST25VF512, SST25VF010A
 - EN25F05, EN25F10

[2,6,7,8,9,10,12,13,14,21,22,23,24,25,27,28,29,34,36,37,39]	+3V
[10,21,23,31,32,33,34,35,36,37,38,39,40]	+5VSUS
[36]	+3VSUS
[33]	+1.1V_VL801

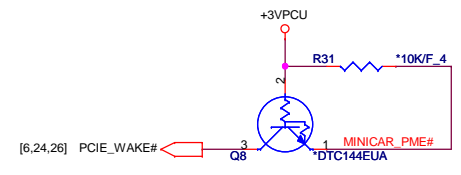
Mini Card WLAN/BT(Optional)



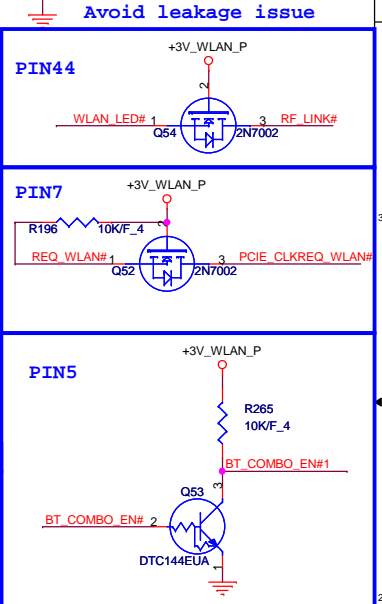
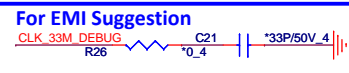
Mini Card Reset



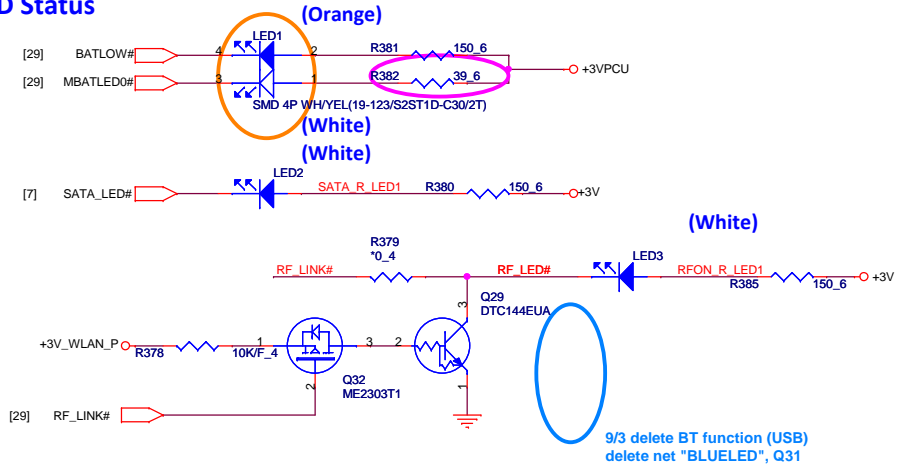
Support Wake Function(Reserve)



LGE mini-pcie power status		
WLAN	Bluetooth	+3V_WLAN_P
Radio-ON	Radio-ON	Power-ON
Radio-ON	Radio-OFF	Power-ON
Radio-OFF	Radio-ON	Power-ON
Radio-OFF	Radio-OFF	Power-ON
Radio-OFF	Radio-OFF	Power-OFF

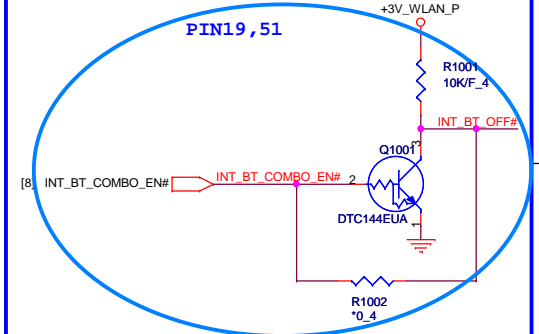


LED Status



MDC Connector(Optional)

- 9/3 delete MDC function
- R538, C570
 - CN15
 - C308, R192, R193, C307, C309, C306, C305
 - "ACZ_SDOUT_MDC"
 - "ACZ_SYNC_MDC"
 - "ACZ_SDIN1"
 - "ACZ_RST#_MDC"
 - "BIT_CLK_MDC"

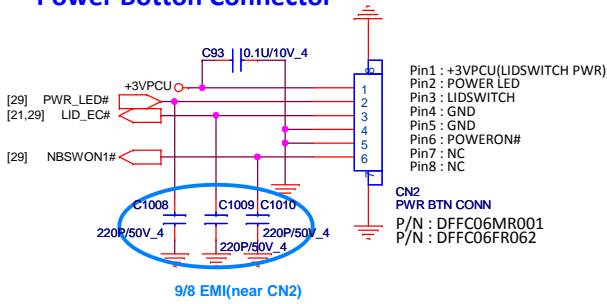


9/4 Intel COMBO card control circuit
1.add R1001,R1002,Q1001
2.add net name "INT_BT_COMBO_EN#" -> "INT_BT_OFF#"

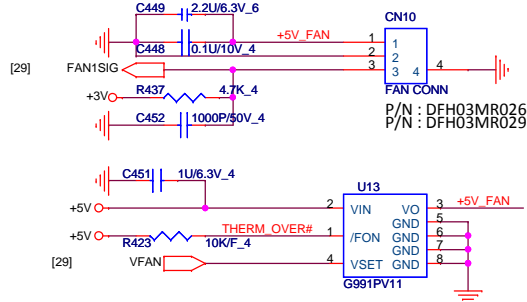
PROJECT : TWH
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Power Button Connector

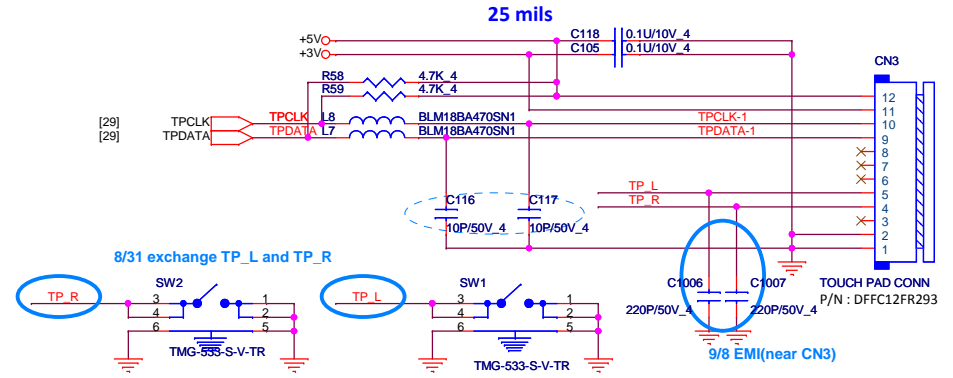


CPU FAN

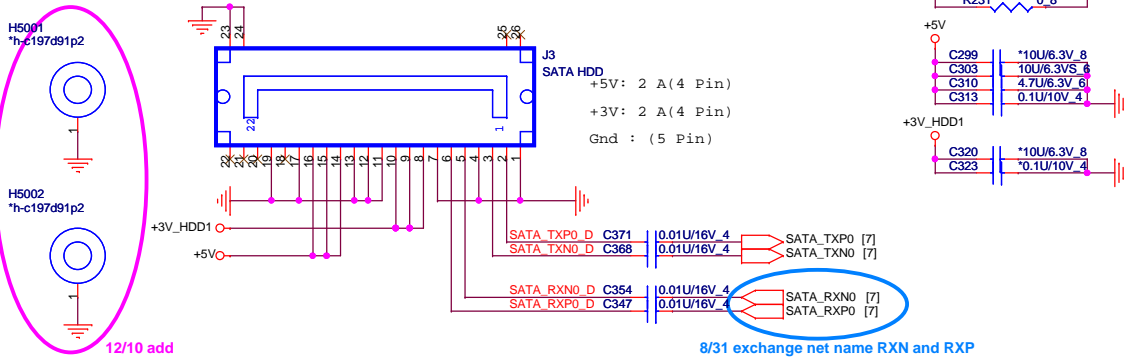


Touch Pad Connector

B-stage change footprint to BL121-12R-TAND-12P-L



SATA HDD Connector

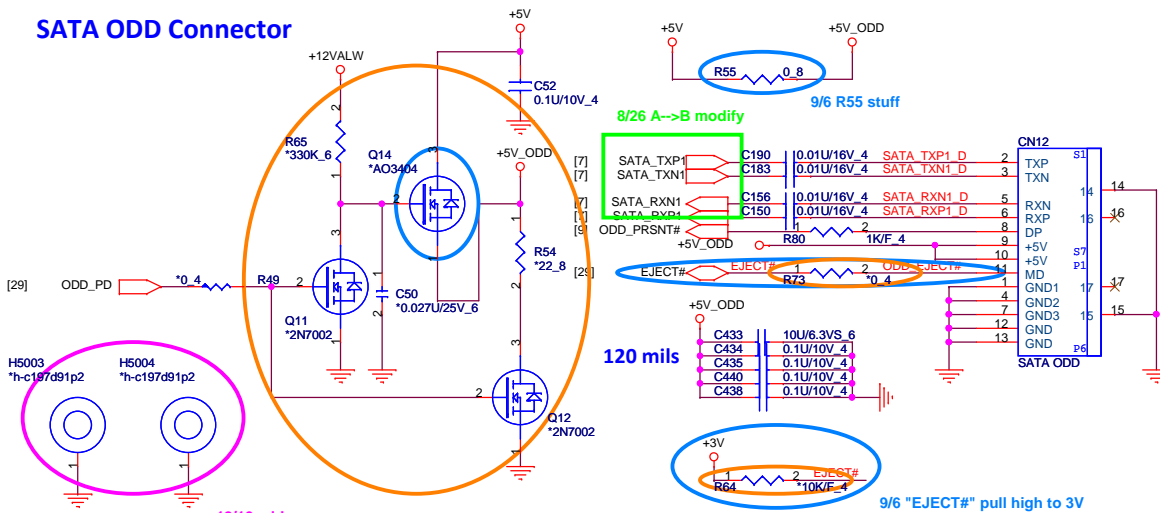


BT Connector

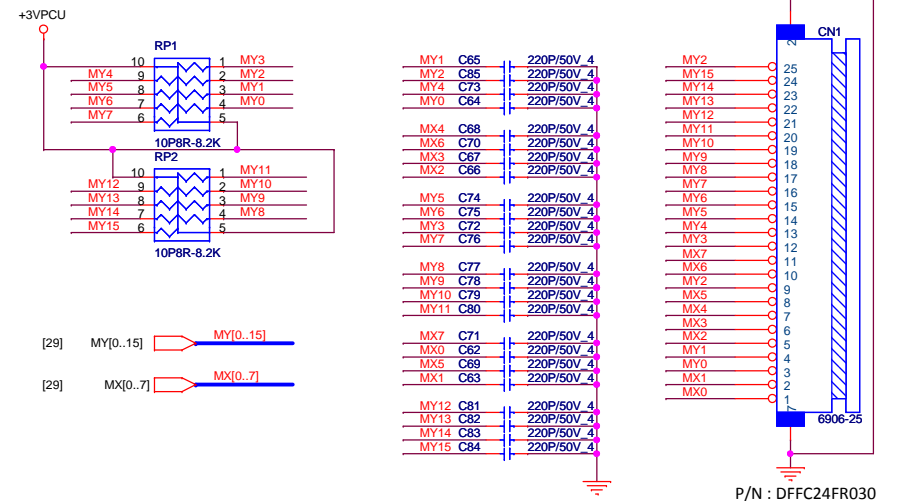


8/31 delete BT function (USB)
 delete CN20, net "BT_OFF#", "BLUELED", "USB8+", "USB8-"

SATA ODD Connector



Keyboard Connector

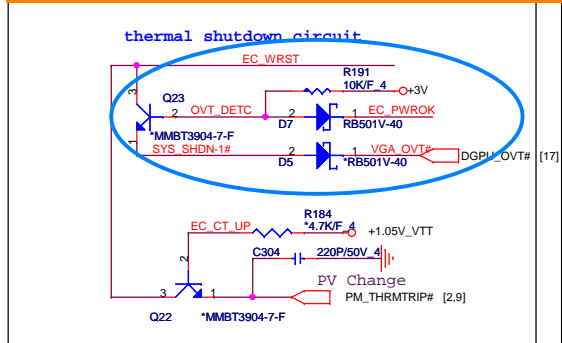
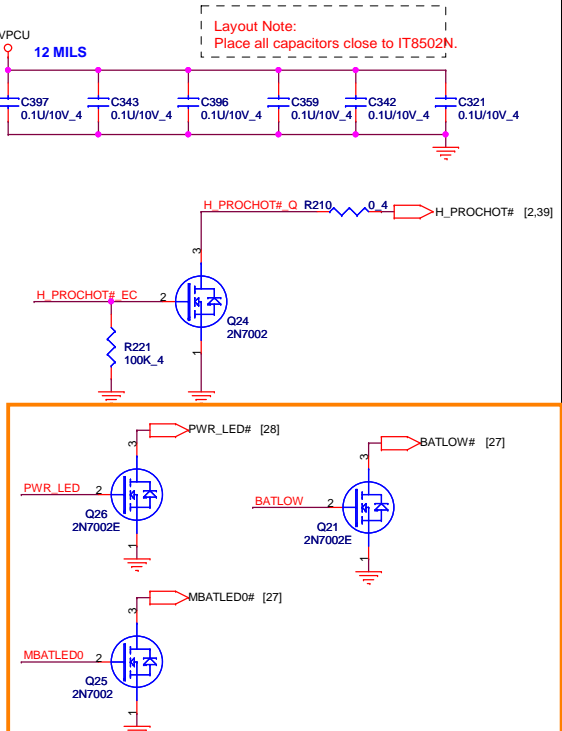
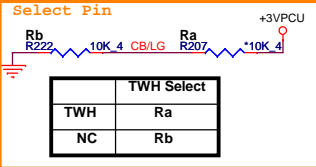
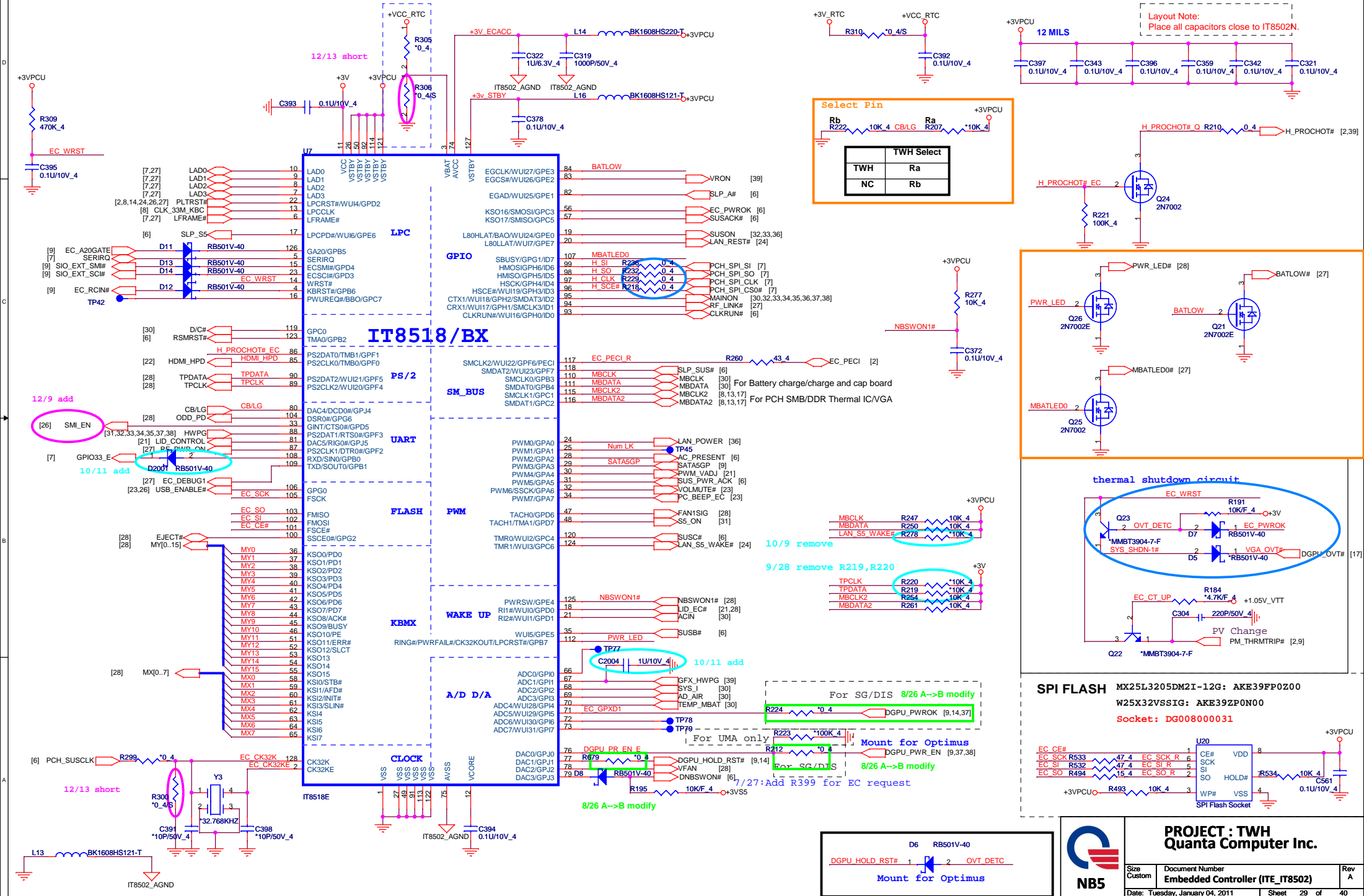


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NB5

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[2,4,10,27] +1.5V_CPU
 [6,7,8,9,10,12,13,14,21,22,23,24,25,26,27,29,34,36,37,39] +3V
 [6,7,10,21,22,23,27,36] +5V

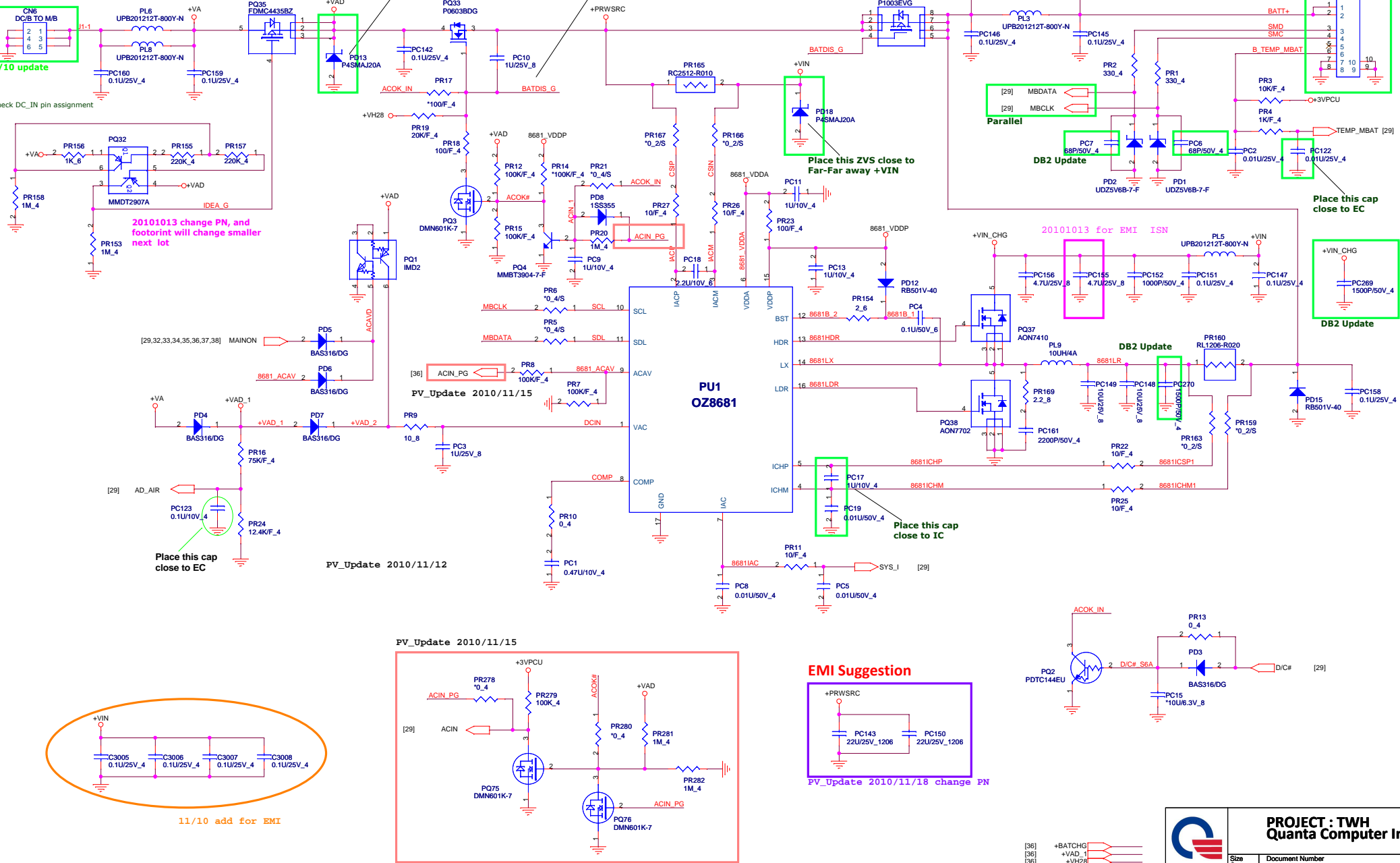


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Mount for Optimus
Mount for Optimus

TOP DC_JACK
65W/90W



CN6
DC/B TO M/B
9/10 update

Check DC_IN pin assignment

20101013 change PN, and
footprint will change smaller
next lot

Place this cap
close to EC

11/10 add for EMI

Place this ZVS close to
idea diode

Do Not add test point on
BATDIS_G signal

Place this ZVS close to
Far-Far away +VIN

Place this cap
close to EC

Parallel
MBDATA
MBCLK

DB2 Update
PC7
88P/50V_4

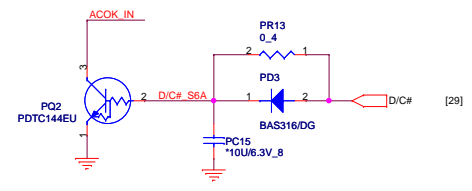
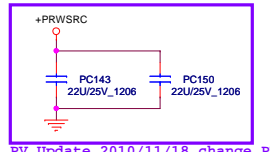
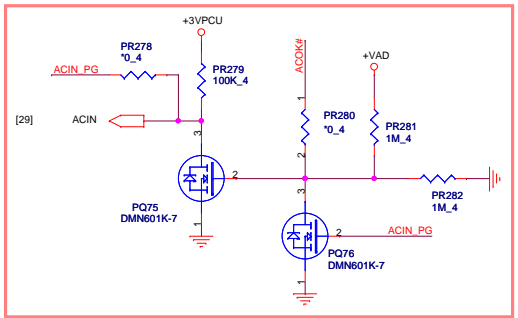
DB2 Update
PC269
1500P/50V_4

Place this cap
close to IC

PV_Update 2010/11/15

EMI Suggestion

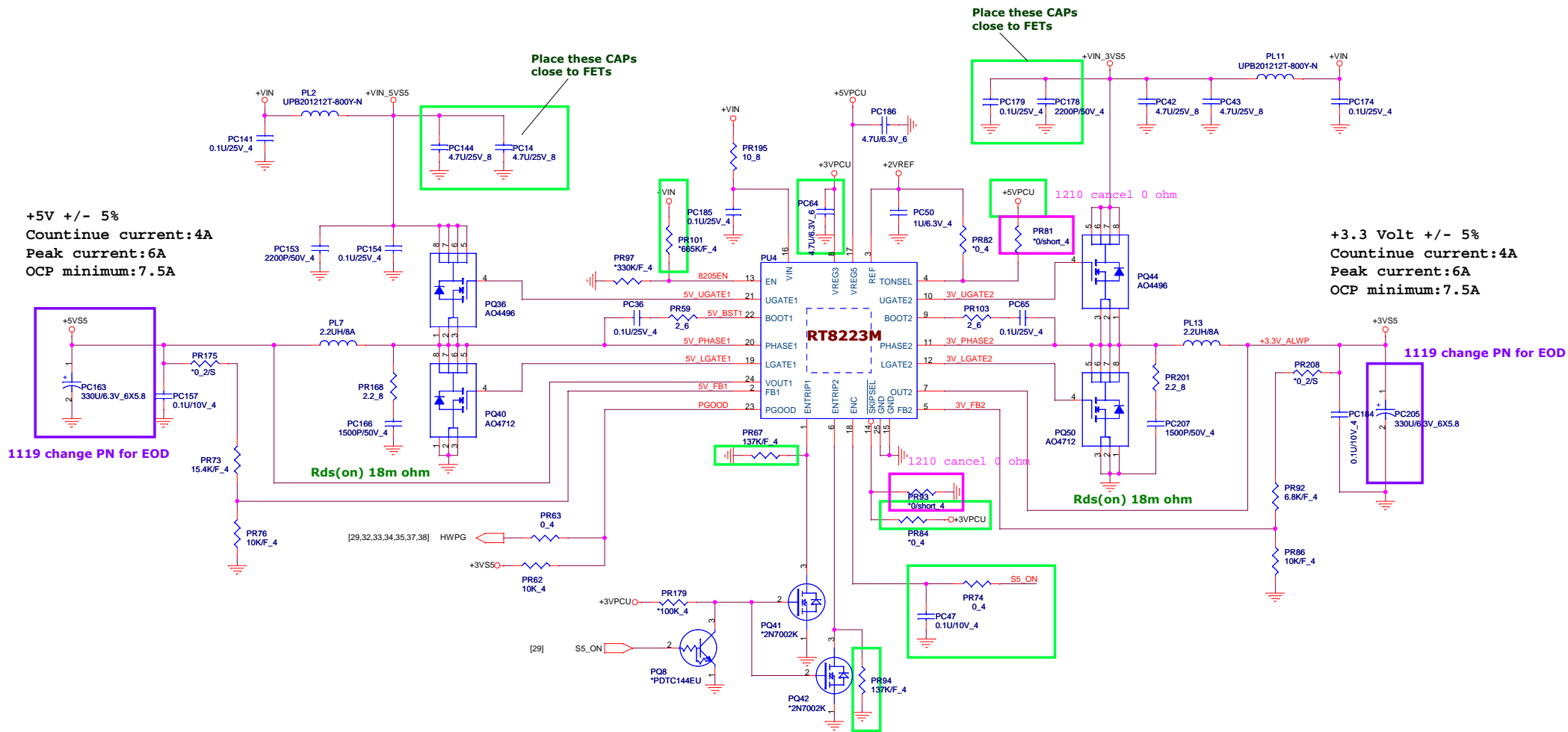
PV_Update 2010/11/18 change PN



- [36] +BATCHG
- [36] +VAD_1
- [36] +VH28
- [36] +VA



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+5V +/- 5%
 Countinue current:4A
 Peak current:6A
 OCP minimum:7.5A

+3.3 Volt +/- 5%
 Countinue current:4A
 Peak current:6A
 OCP minimum:7.5A

1119 change PN for EOD

Rds(on) 18m ohm

Rds(on) 18m ohm

1119 change PN for EOD

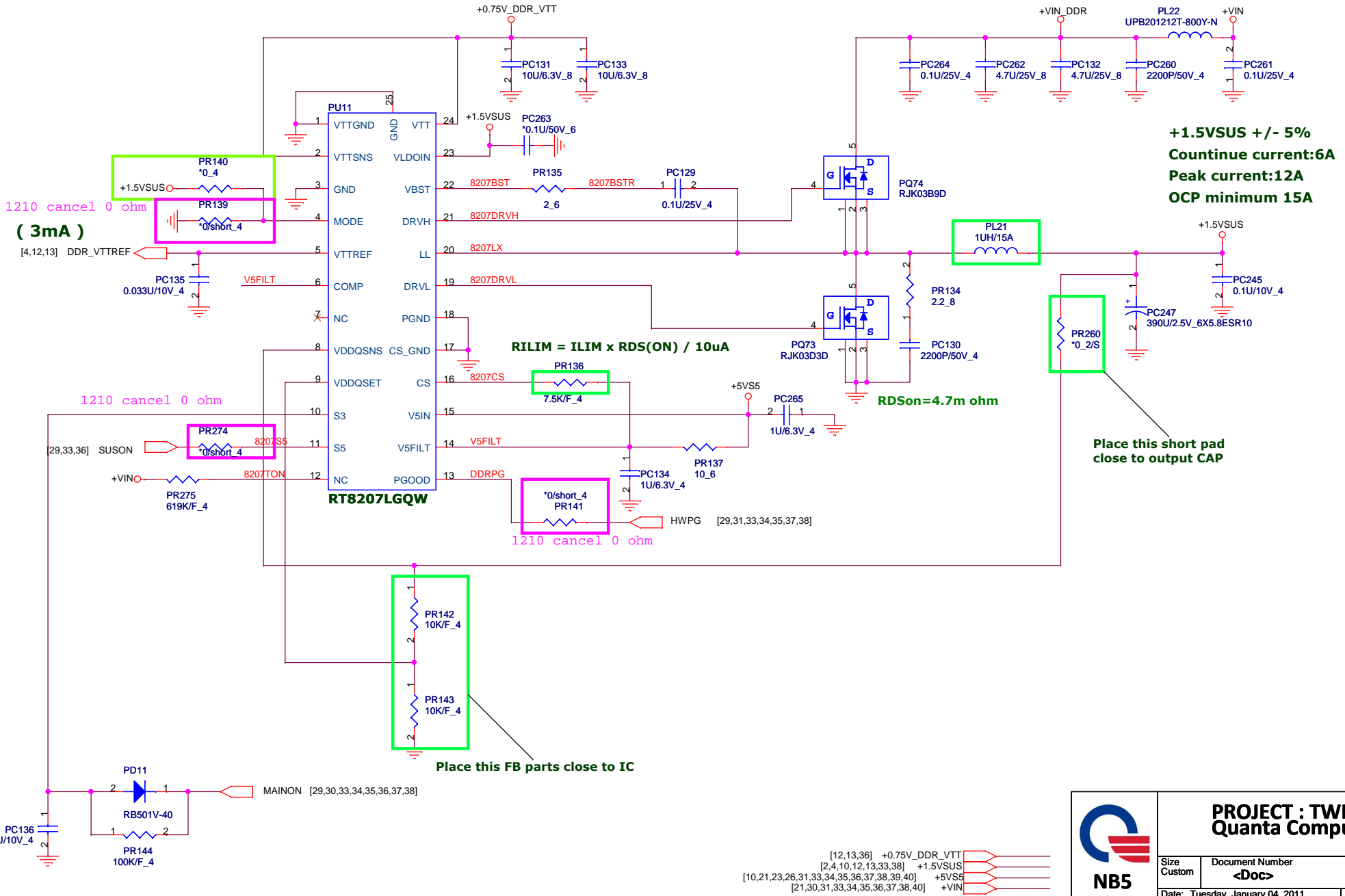
Place these CAPS close to FETS

Place these CAPS close to FETS

+5VPCU

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(VTT/2A)



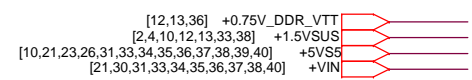
+1.5VSUS +/- 5%
Continue current: 6A
Peak current: 12A
OCp minimum 15A

$$RILIM = ILIM \times RDS(ON) / 10\mu A$$

RDSon=4.7m ohm

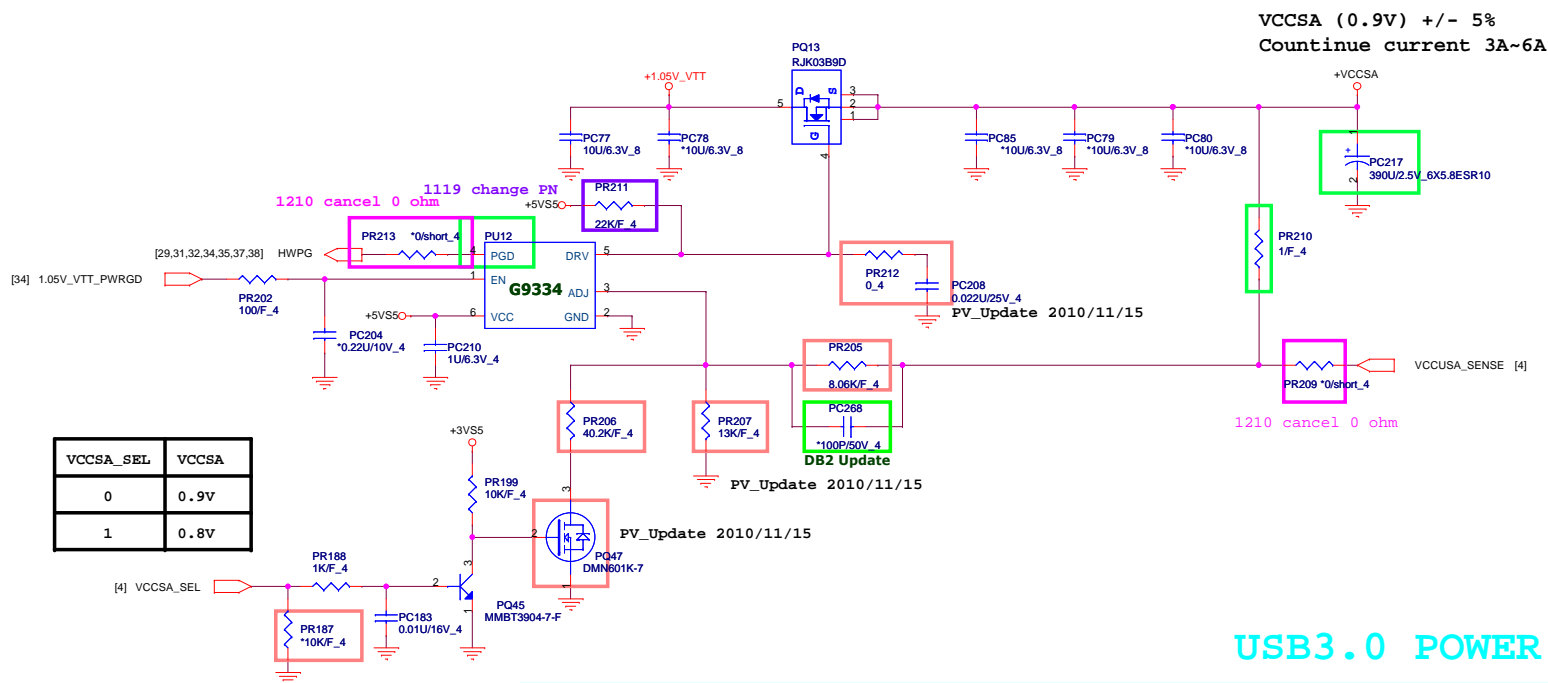
Place this short pad close to output CAP

Place this FB parts close to IC

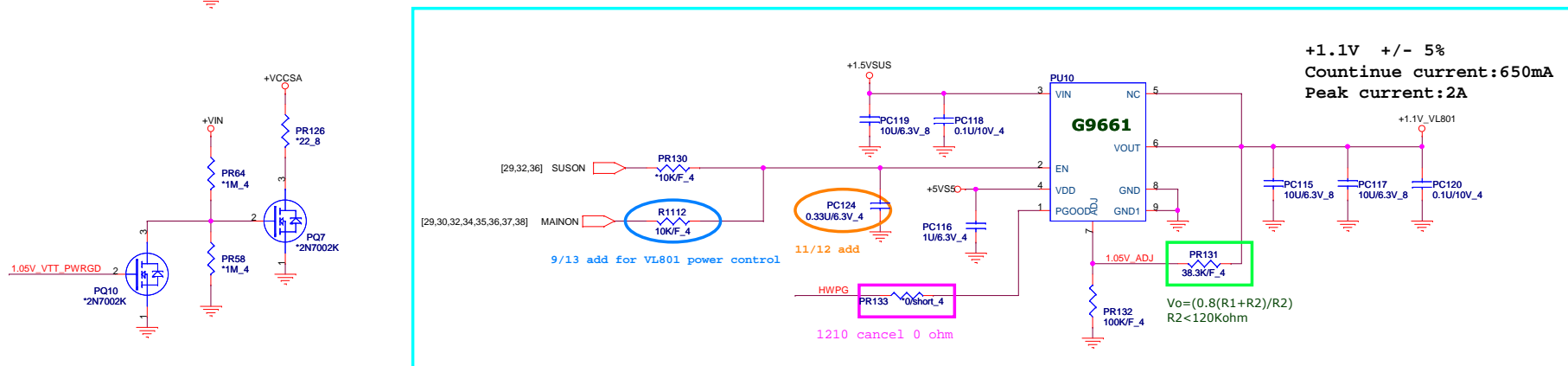


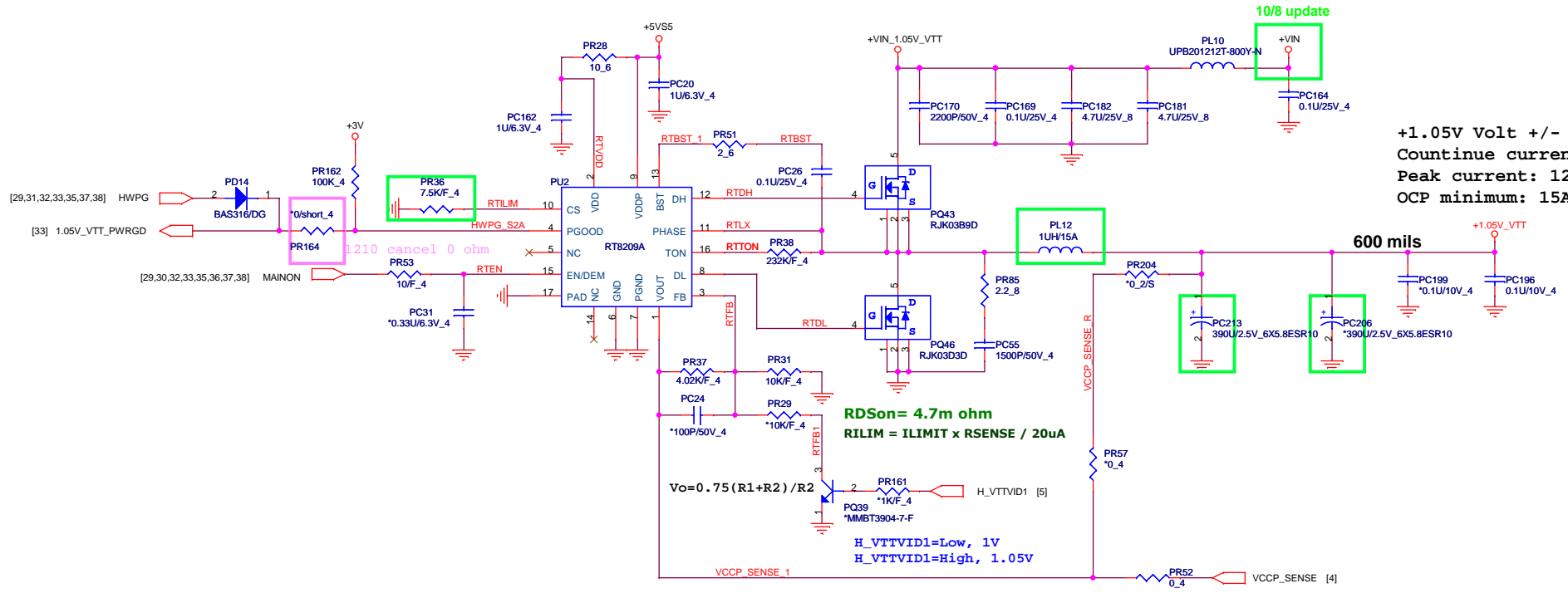
PROJECT : TWH
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USB3.0 POWER





+1.05V Volt +/- 5%
 Countinue current:10A
 Peak current: 12A
 OCP minimum: 15A

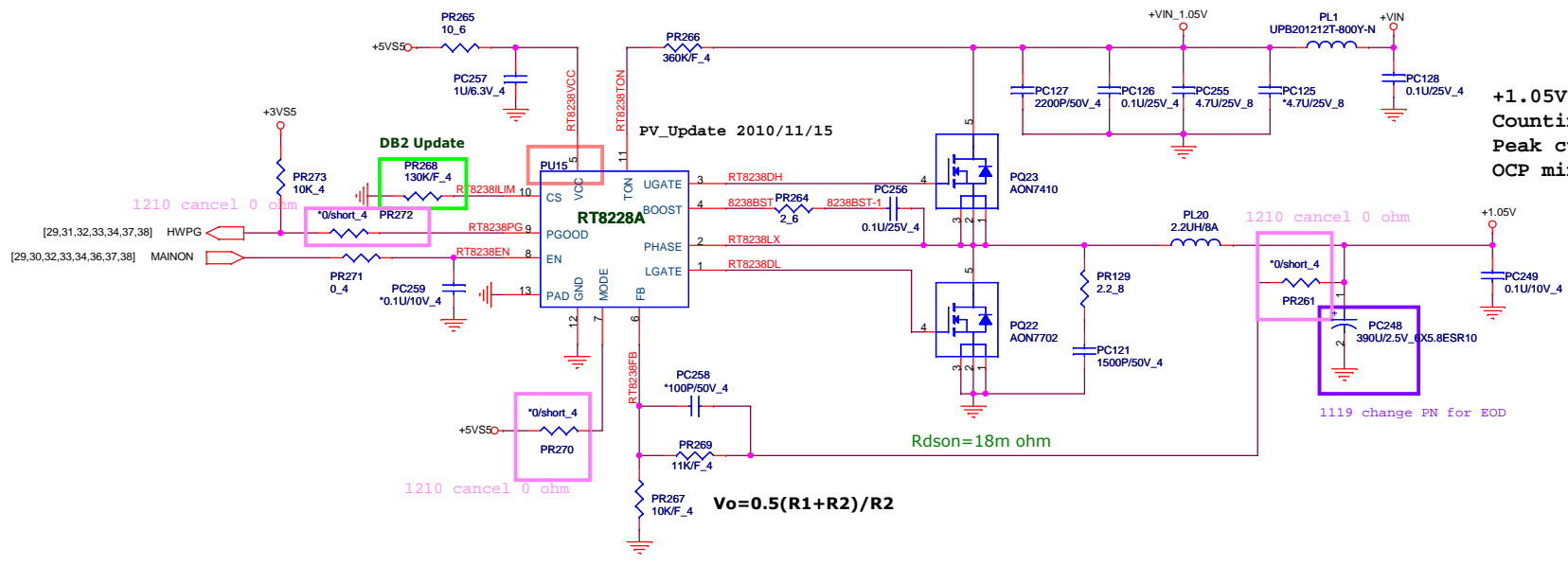
RD_{son} = 4.7m ohm
RILIM = ILIMIT x RSENSE / 20uA

V_o = 0.75 (R1+R2) / R2
H_VTTVID1=Low, 1V
H_VTTVID1=High, 1.05V



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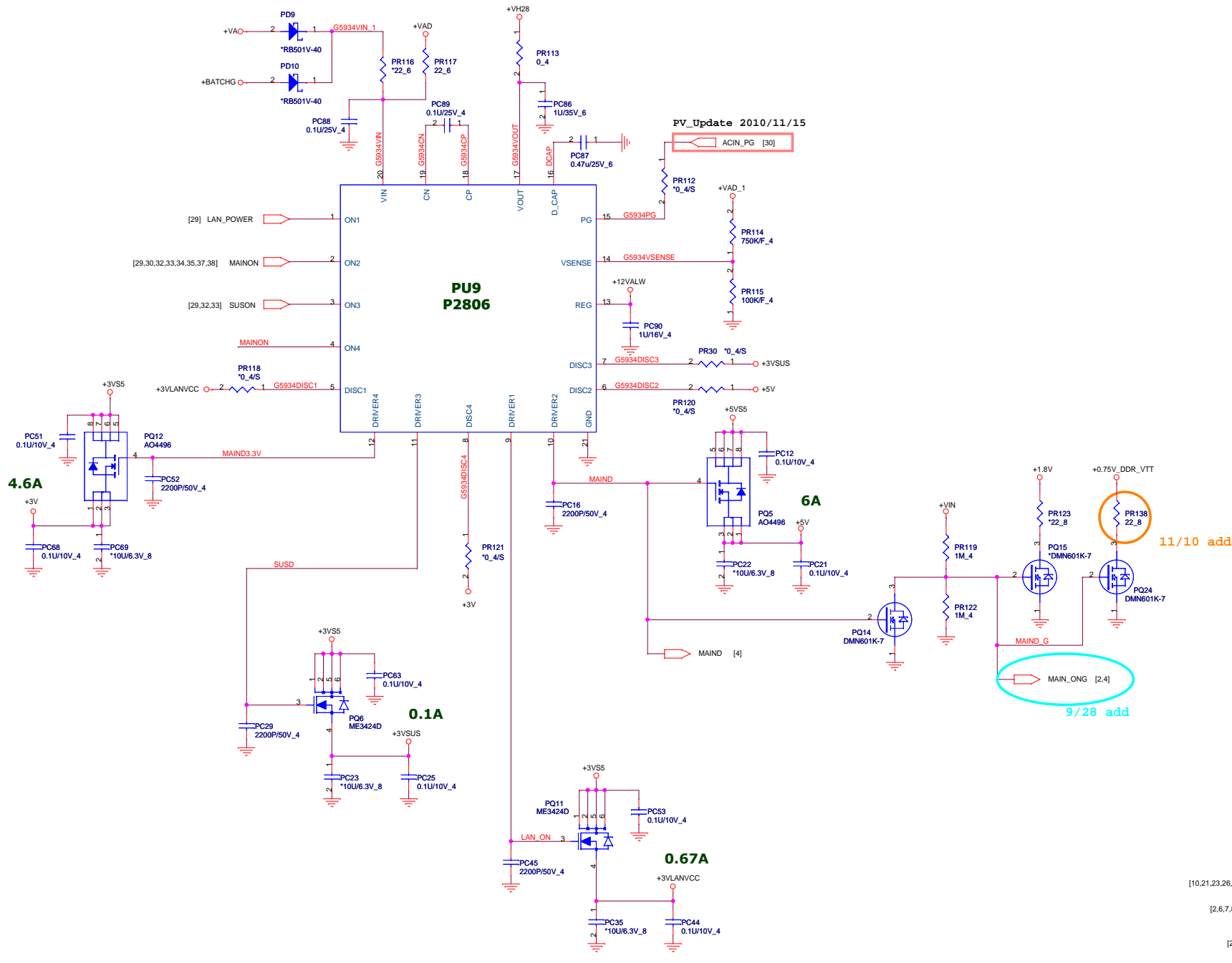
+1.05V +/- 5%
Countinue current:6A
Peak current: 8A
OCP minimum: 10A

$V_o = 0.5(R1 + R2) / R2$



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[12,13,32]	+0.75V_DDR_VTT
[24]	+3VLANVCC
[2,4,10,12,13,32,33,38]	+1.5VSUS
[30]	+BATCHG
[21,28,38]	+12VALW
[10,21,23,26,31,32,33,34,35,37,38,39,40]	+5VS5
[2,6,7,8,9,10,14,24,29,31,33,35,38]	+3VS5
[30]	+VAD_1
[30]	+VH28
[4,7,10,38]	+1.8V
[21,30,31,32,33,34,35,37,38,40]	+VIN
[6,7,10,21,22,23,27,28]	+5V
[30]	+VA

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Quanta Computer Inc.

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ciucuit default is N12P

VGA type	PQ17 PQ19 PQ16 PQ18	PR252
N12E	POP (SMT)	1.37K
N12P	NA (no SMT)	806 ohm (CS18062FB29)

Nvideo N12E

CNTRL1	CNTRL0	N11E-GE
GPIO6	GPIO5	
0	0	0.9125V
0	1	0.8625V
1	0	0.8125V
1	1	N/A

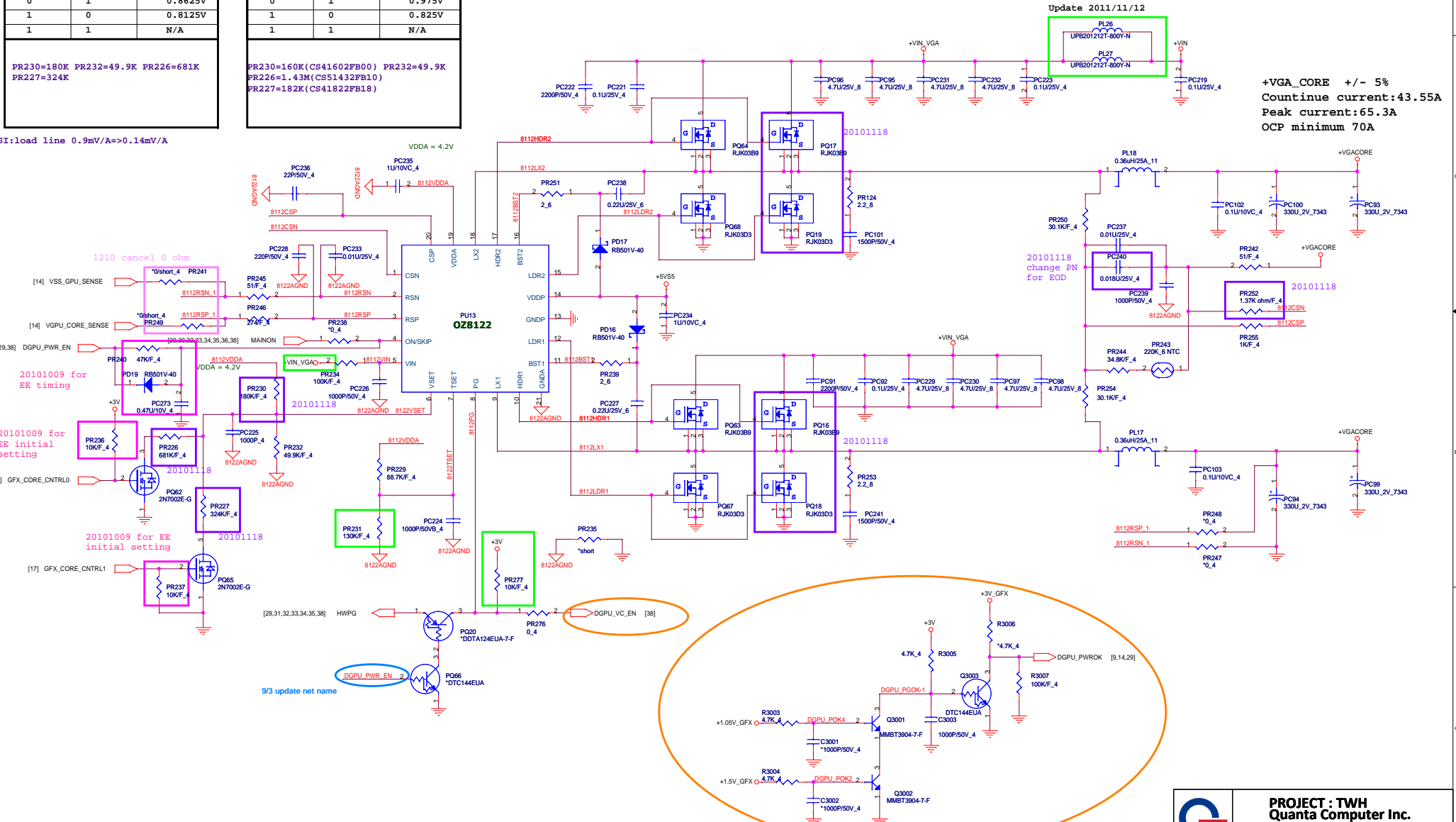
PR230=180K PR232=49.9K PR226=681K
PR227=324K

Nvideo N12P

CNTRL1	CNTRL0	N11E-GE
GPIO6	GPIO5	
0	0	1V
0	1	0.975V
1	0	0.825V
1	1	N/A

PR230=160K (CS41602FB00) PR232=49.9K
PR226=1.43M (CS51432FB10)
PR227=182K (CS41822FB18)

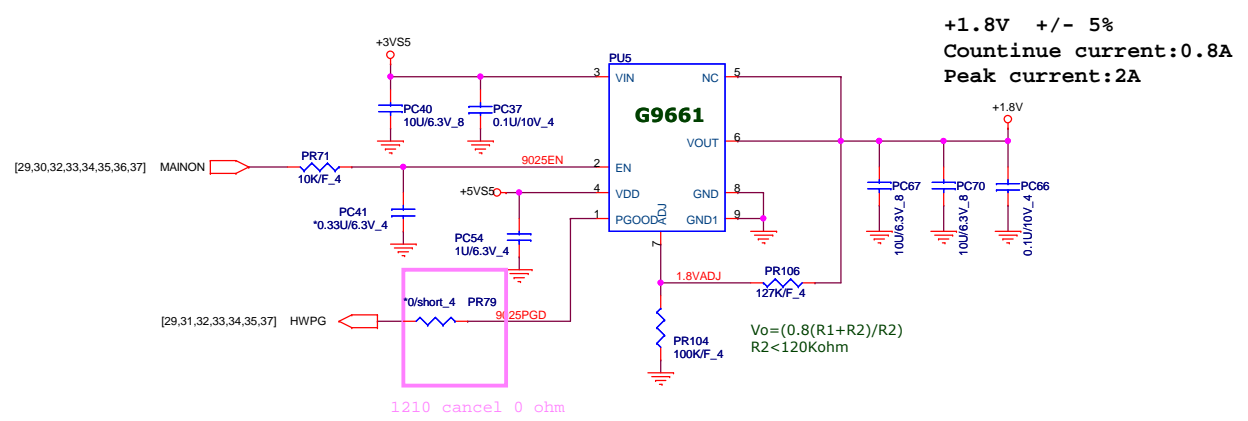
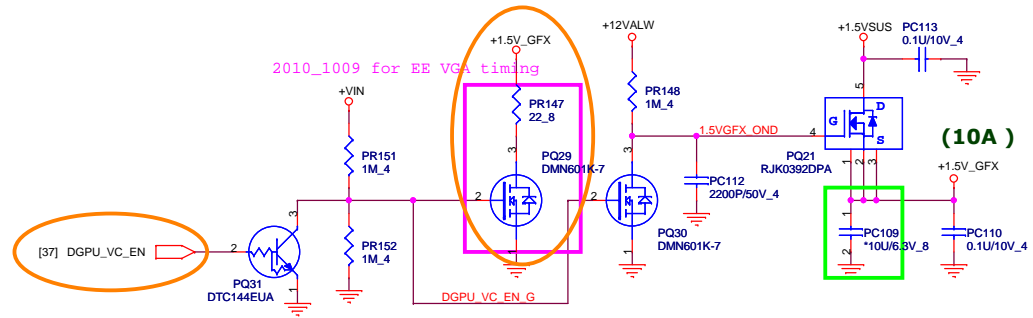
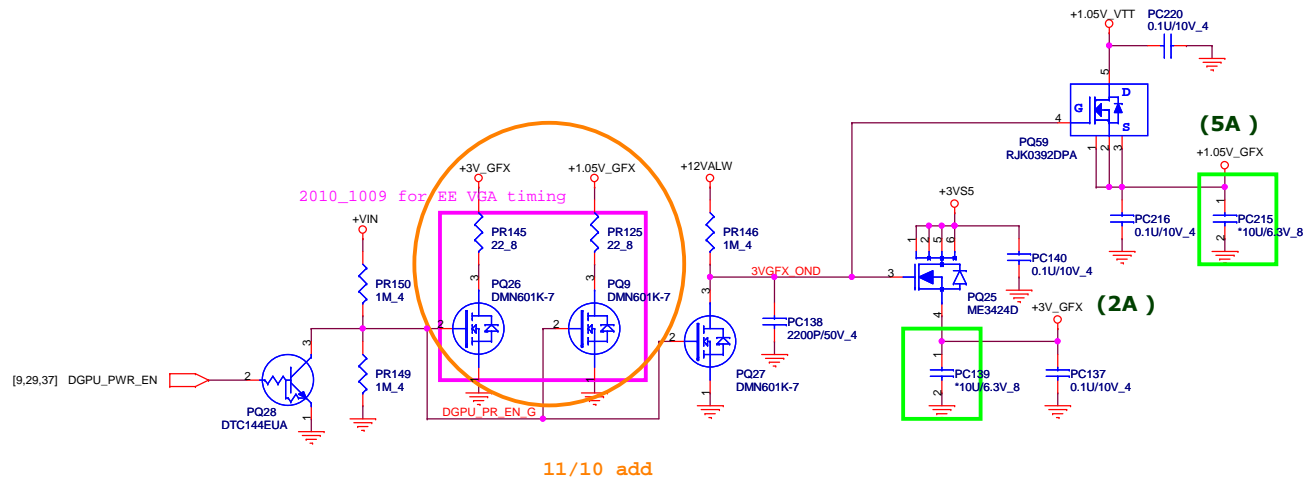
SI:load line 0.9mV/A=>0.14mV/A



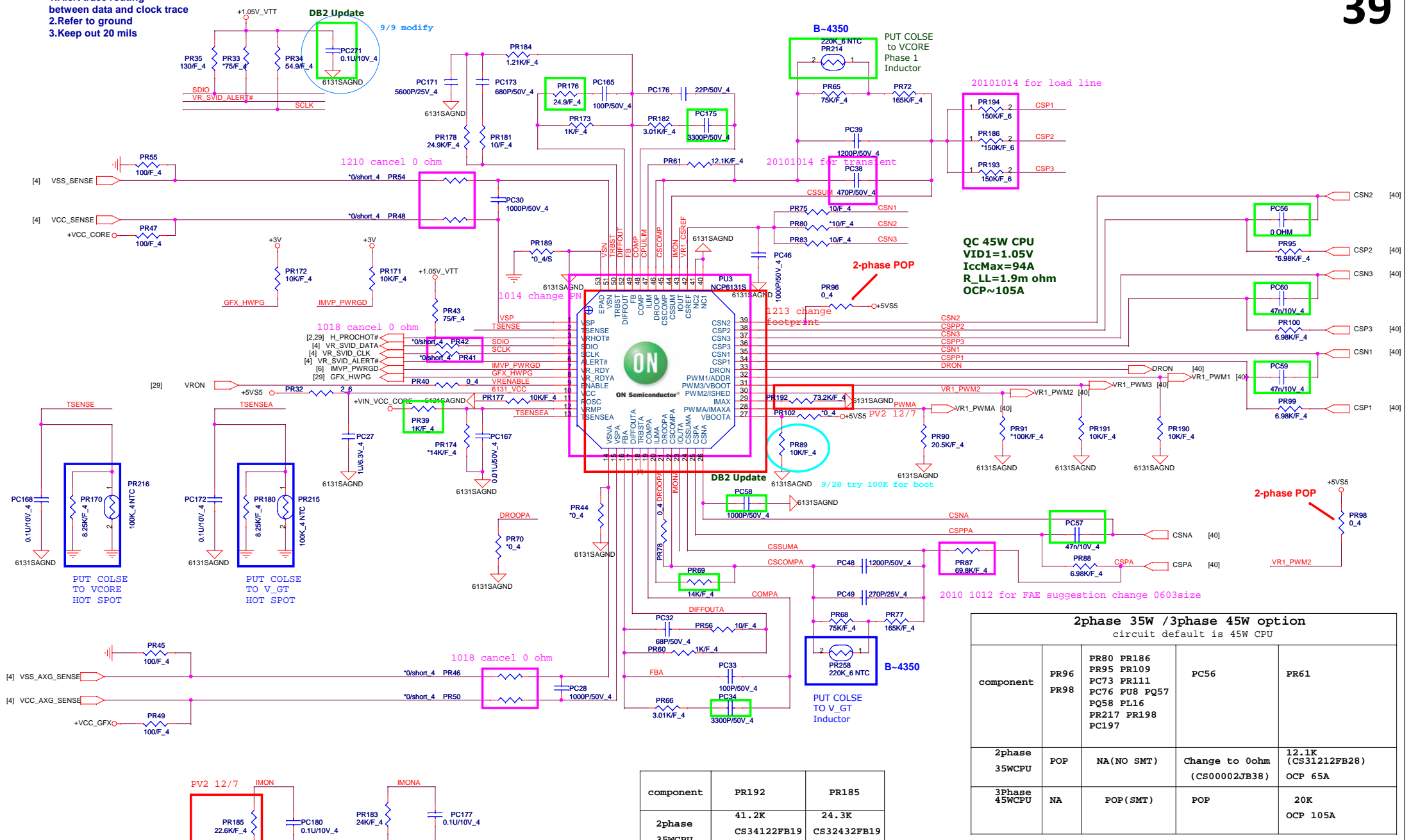
+VGA_CORE +/- 5%
Continue current: 43.55A
Peak current: 65.3A
OCP minimum 70A

11/10 add for DGPU_PWROK circuit

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- 1.Alert trace routing between data and clock trace
- 2.Refer to ground
- 3.Keep out 20 mils



QC 45W CPU
VID1=1.05V
IccMax=94A
R_LL=1.9m ohm
OCP~105A

2phase 35W /3phase 45W option
circuit default is 45W CPU

component	PR96 PR98	PR80 PR186 PR95 PR109 PC73 PR111 PC76 PU8 PQ57 PQ58 PL16 PR217 PR198 PC197	PC56	PR61
2phase 35WCPU	POP	NA(NO SMT)	Change to 0ohm (CS00002JB38)	12.1K (CS31212FB28) OCP 65A
3Phase 45WCPU	NA	POP(SMT)	POP	20K OCP 105A

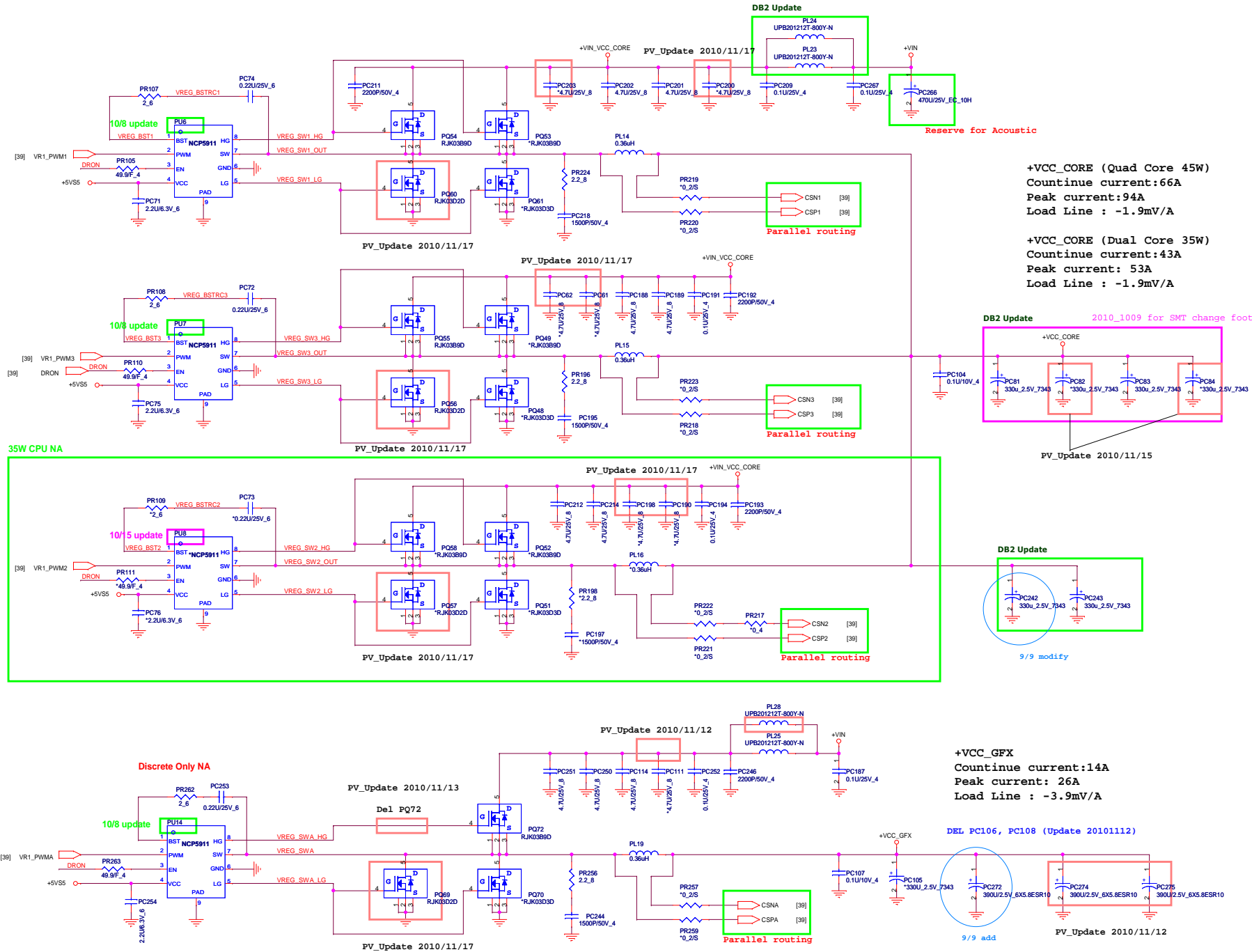
component	PR192	PR185
2phase 35WCPU	41.2K CS34122FB19	24.3K CS32432FB19
3Phase 45WCPU	73.2K CS37322BB00	22.6K CS32262FB15

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NBS

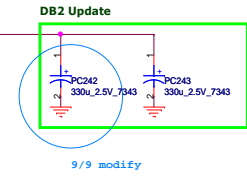
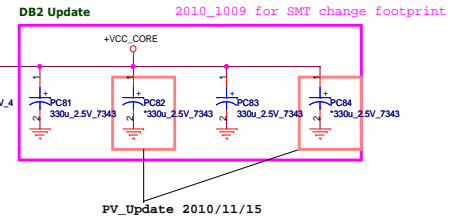
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+VCC_CORE (Quad Core 45W)
 Countinue current:66A
 Peak current:94A
 Load Line : -1.9mV/A

+VCC_CORE (Dual Core 35W)
 Countinue current:43A
 Peak current: 53A
 Load Line : -1.9mV/A



+VCC_GFX
 Countinue current:14A
 Peak current: 26A
 Load Line : -3.9mV/A

